Open-Q™ 660 HDK Hardware Development Kit based on the Snapdragon™ 660 processor User Guide

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IDENTIFICATION

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1.0	October 24, 2017	Initial Draft	All

Table of Contents

1. INTRODUCTION

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 660 HDK Hardware Development Kit based on the Snapdragon™ 660 processor.

For more background information on this development kit, visit: www.intrinsyc.com

1.2 Scope

This document will cover the following items on the Open-Q 660 Hardware Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- Processor board
- Carrier Board
- Display Board for LCD (Optional)

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Intrinsyc Open-Q 660 Hardware Development Kit.

2. DOCUMENTS

This section lists the supplementary documents for the Open-Q 660 Hardware Development Kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

REFERENCE	TITLE

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter

UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3. OPEN-Q 660 HARDWARE DEVELOPMENT KIT

3.1 Introduction

The Open-Q 660 Hardware Development Kit provides a quick reference or evaluation platform for Qualcomm's Snapdragon™ 660 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® Snapdragon™ 660 series technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 660 Hardware Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 660 Hardware Development Kit includes the following:

- Open-Q 660 Processor board with the Snapdragon™ 660 (SDA660) processor main CPU board
- Mini-ITX form-factor carrier board for I/O and connecting with external peripherals
- 12V power adapter
- USB type-C cable and charger

- 5.7” (1080x1920) AMOLED Display card (Additional Accessory)
- Lithium ion battery 4.4V/3000mAh (Additional Accessory)

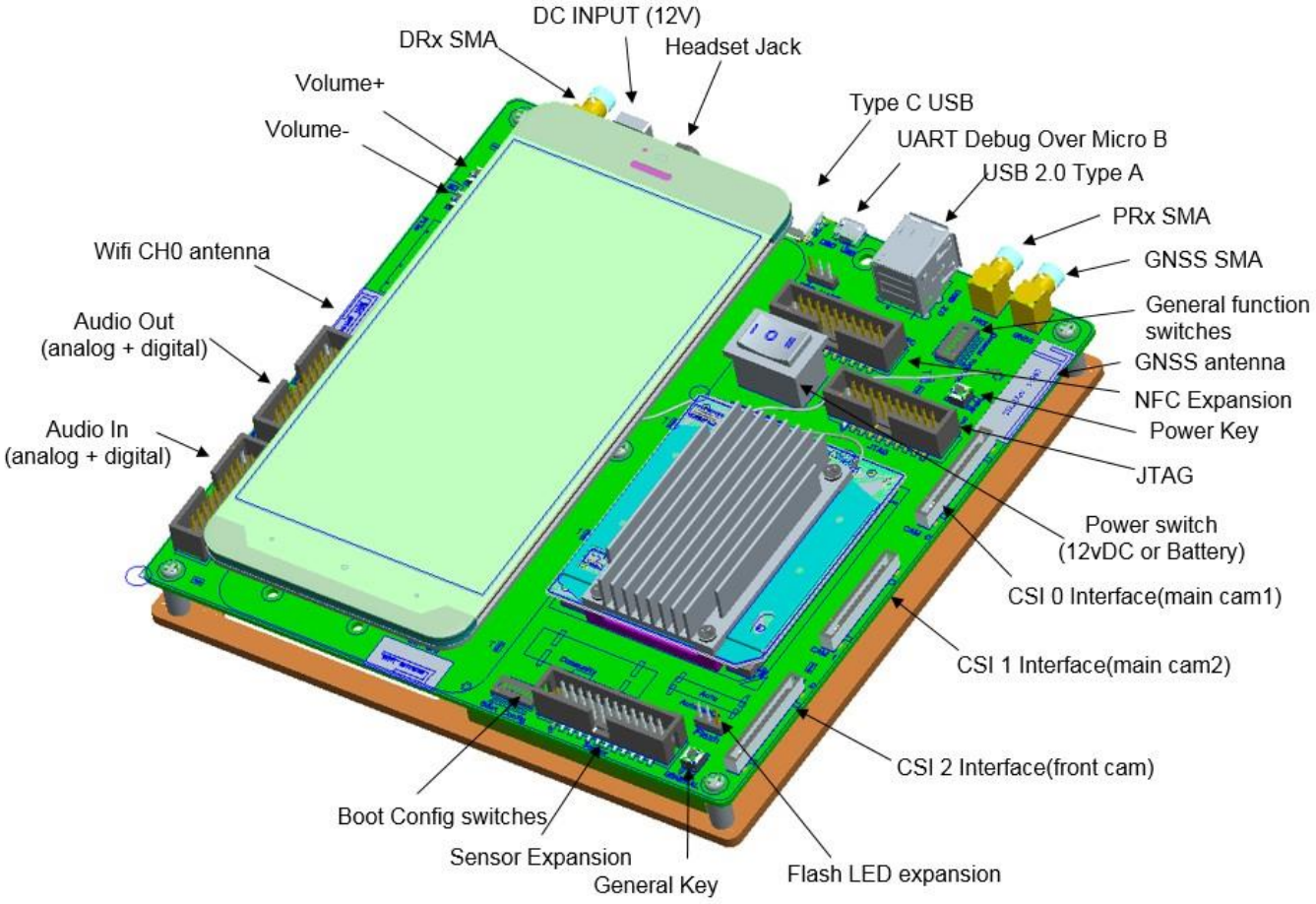

Figure 1 Assembled Open-Q 660 Hardware Development Kit top

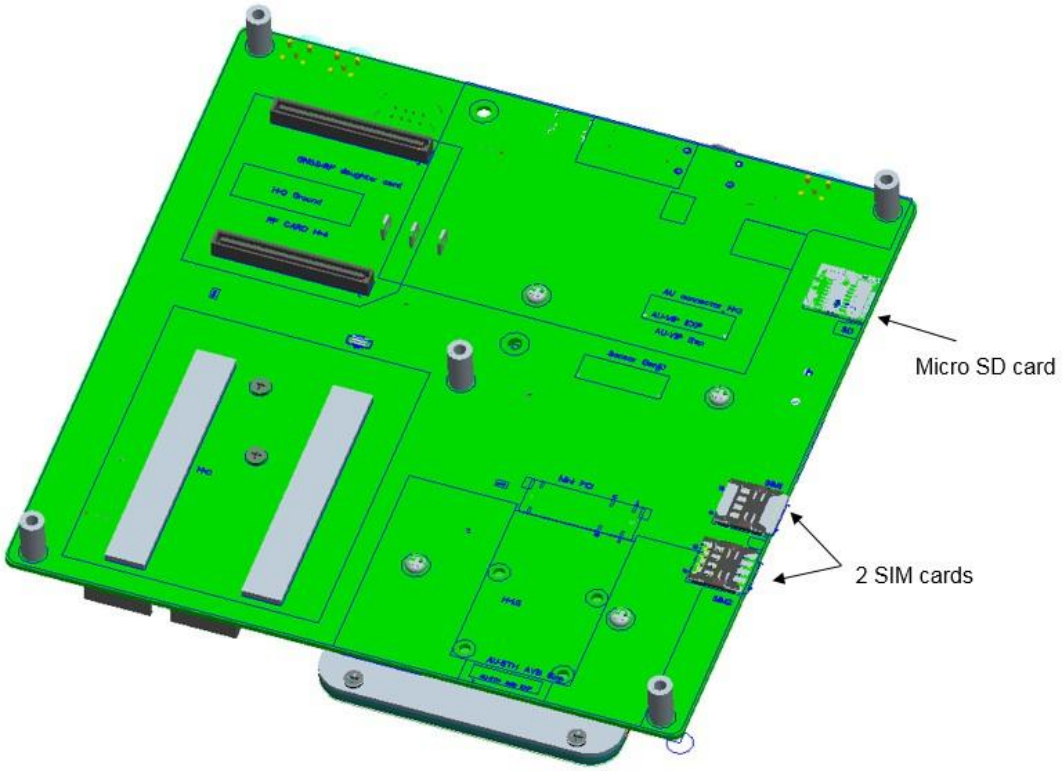

Figure 2 Assembled Open-Q 660 Hardware Development Kit bottom

The development kit comes with Android software pre-programmed on the CPU board or processor board. Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: sales@intrinsyc.com

3.5 Hardware Identification Label

Labels are present on the CPU board. The following information is conveyed on these two boards:

Processor board:

- Serial Number
- WIFI MAC address

Refer to http://support.intrinsyc.com/account/serialnumber for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: http://support.intrinsyc.com/account/register

Note: Please retain the and carrier board serial number for warranty purposes.

3.6 System Block Diagram

The following diagram explains the interconnectivity and peripherals on the development kit.

The following diagram explains the interconnectivity and peripherals on the development kit.

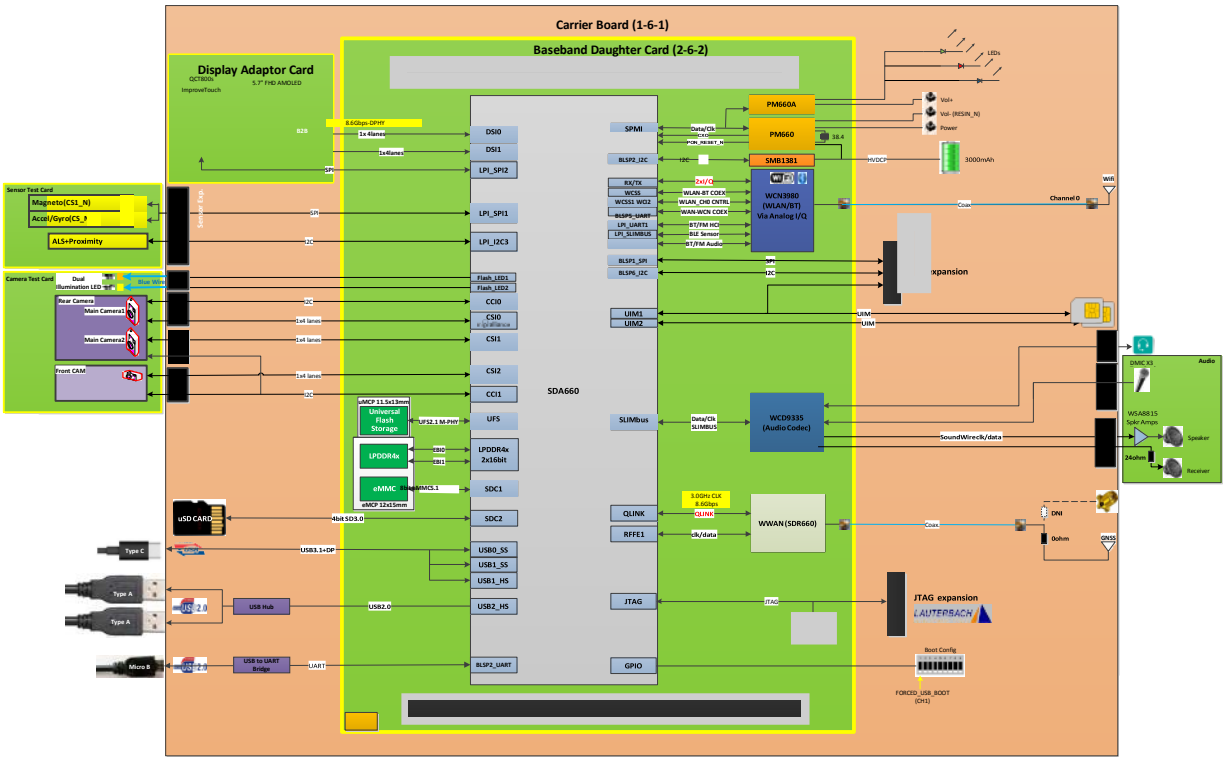

Figure 3 Open-Q 660 Processor board + Carrier Board Block Diagram

3.7 Open-Q 660 Processor Board

The Processor board provides the basic common set of features with minimal integration efforts for end users. It contains the following:

- Snapdragon 660 (SDA660) main application processor
- Memory (eMCP/uMCP compatible design)
    - Note: eMCP is the only configuration available from Intrinsyc
- eMCP: 64GB eMMC 5.1 + LPDDR4x up to 1866MHz 6GB RAM
- uMCP: 128GB UFS 2.1 + LPDDR4x up to 1866MHz 6GB RAM
- PMIC: PM660 + PM660A – PMIC for Peripheral LDOs, Boost Regulators
- WCN3980 Atheros Wi-Fi + BT +FM combo chip over SLIMbus, Analog IQ, UART, PCM
- WCD9335 Audio Codec
- SDR660 GNSS support

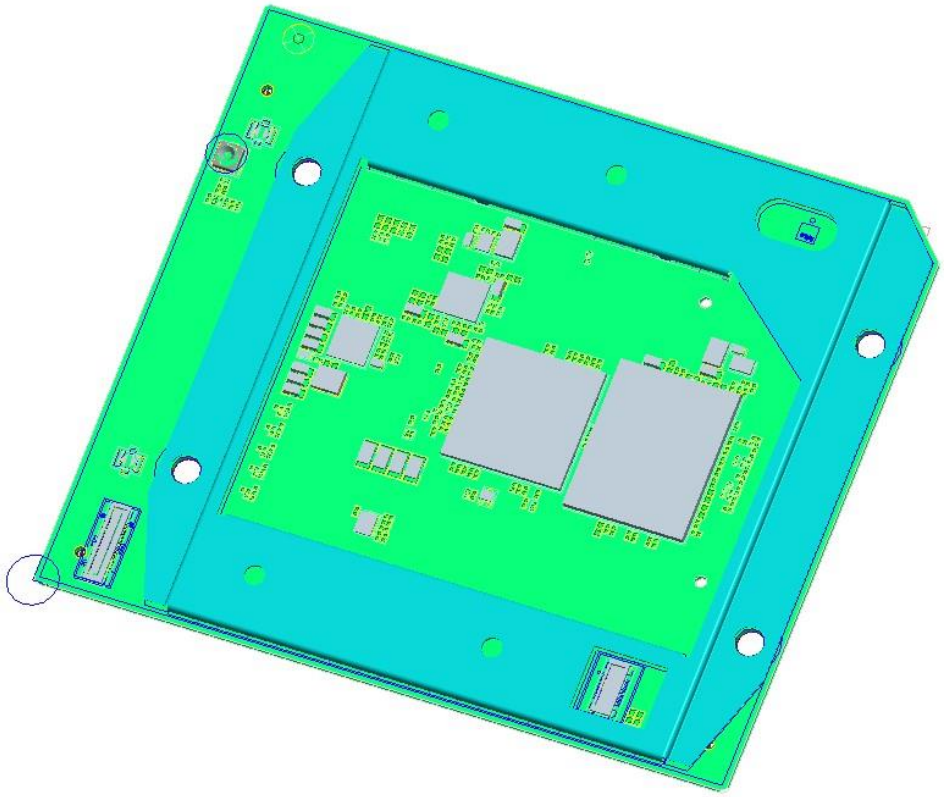

Figure 4 Open-Q 660 PROCESSOR BOARD

3.7.1 Processor Board Mechanical Properties

Table 3.7-1 Open-Q 660 Processor Board Mechanical Properties

Area	42 cm^2(60 mm x 70 mm)
Interface	2 x 240-pin high speed board to board connectors.
Thermal	A top side heat sink and a bottom side heat conductive metal plate are installed by default.

3.7.2 Processor Board Block Diagram

The Open-Q 660 Processor board measuring 60mm x 70mm is where all the processing occurs. It is connected to the carrier via two 240-pin high speed board-to-board connector. The purpose of the connectors is to bring out essential signals such that other peripherals can interface with the platform.

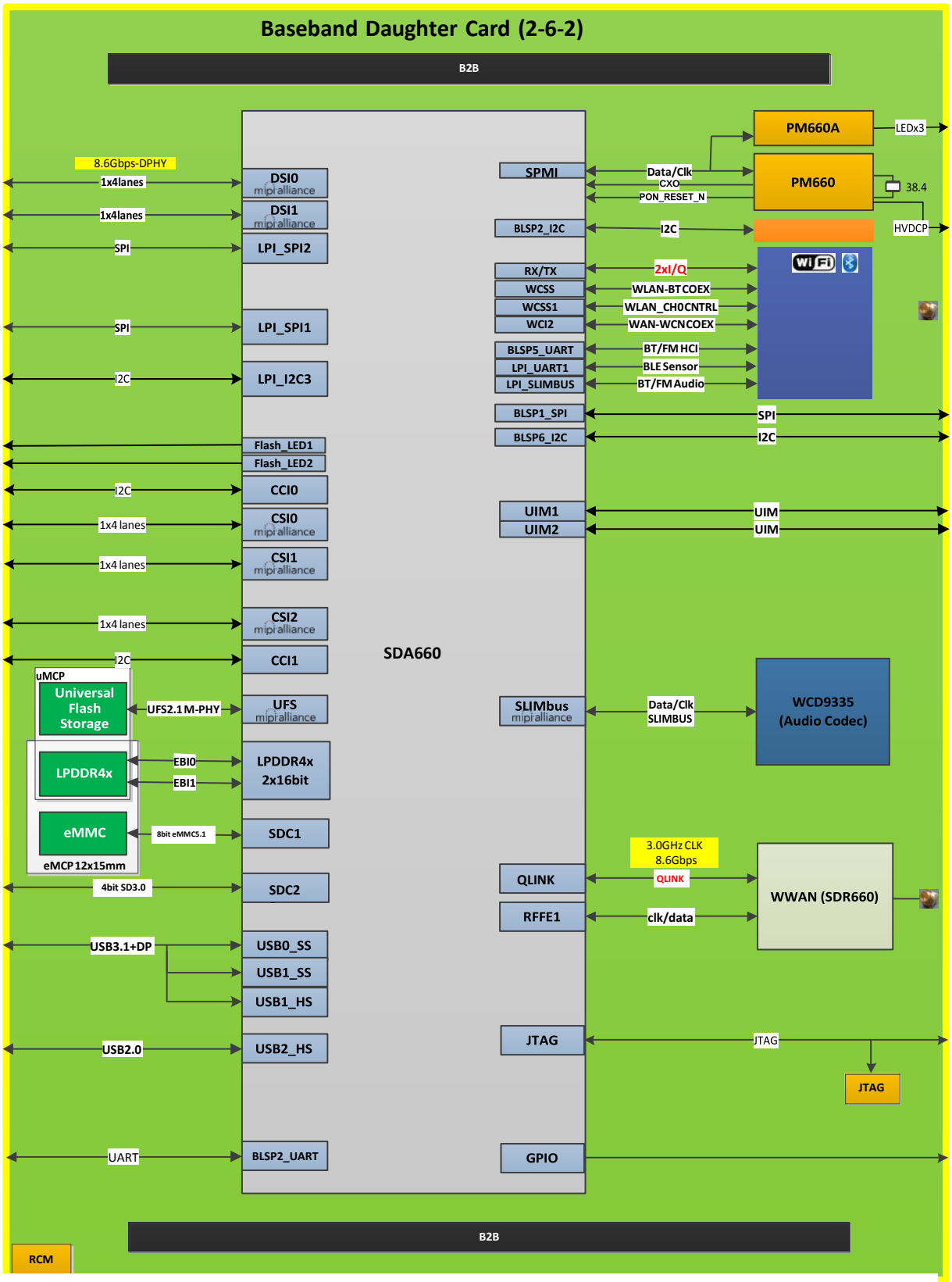

Figure 5 Open-Q 660 Processor Board Block Diagram

3.7.3 Hardware Specification

Table 3.7-2 Open-Q 660 Processor Board Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	SDA660	Qualcomm® Snapdragon™ 660 Processor	Qualcomm® Kyro CPU, quad core, 64-bit ARM V8 compliant processor, 2.2GHz
	PMIC (PM660 & PM660A)	Qualcomm® PMIC, Companion PMIC for SDA660 processor	NA
Memory	eMCP	64GB eMMC + 6GB LPDDR4X	eMMC 5.1+ LPDDR4x up to 1866MHz
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via WCN3980WCN3980 – Analog IQ, WSI 2.0,	Wi-Fi Atheros WCN3980WCN3980 Wi-Fi + BT +FM Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via WCN3980WCN3980 over analog IQ, WSI 2.0,
	BT 2.4 GHz via WCN3980WCN3980 – UART / SLIMbus	Wi-Fi Atheros WCN3980WCN3980 Wi-Fi + BT +FM Combo Chip	Support BT 5.0 + HS and backward compatible with BT 1.x, 2.x + EDR
	GNSS via SDR660 –Qlink Qualcomm Proprietary Protocol	GNSS Frontend	GNSS/ GLONASS/ COMPASS/Galilei
RF	2xWLAN / BT	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
	1x GNSS	Connect to antenna on carrier board via coax cable	GNSS/ GLONASS/ COMPASS /Galilei
Audio	1 x Headset Output	Headset/ headphone output	Analog differential output
	2 x Loud-speaker	2 x loud-speaker output	Digital output
	1 x Earpiece output	Earpiece output	Analog differential output
	3 x analog MICs	Analog MIC input	Analog differential input
	3 x digital MICs	Digital MIC input	Digital input
Camera	3 x MIPI CSI	Camera Connectors CSI0, CSI1, CSI2	MIPI Alliance Specification v1.2
Display	1 x MIPI DSI (DSI0 & DSI1) + Touch 100-pin display Connector	100- pin display connector	MIPI Alliance Specification v1.2. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01 ,v1.2
USB	1 x Type-A USB 2.0 HOST 1 x Type-C USB 3.1	Type-A USB 2.0 HOST Type-C USB 3.1	USB2.0 USB3.1
Connectors	2 x 240pin Carrier board connector	Connector for Carrier board	2 x 240 pin B2B connector

3.8 Open-Q 660 Carrier Board

The Open-Q 660 Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

Table 3.8-1 Open-Q 660 Carrier Board Mechanical Properties

Dimensions	289 cm^2 (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	Carrier board: 2x240 pin board to board connector Display: 100 pin board to board connector
Thermal	Thermal pad is placed between the Carrier board and carrier board

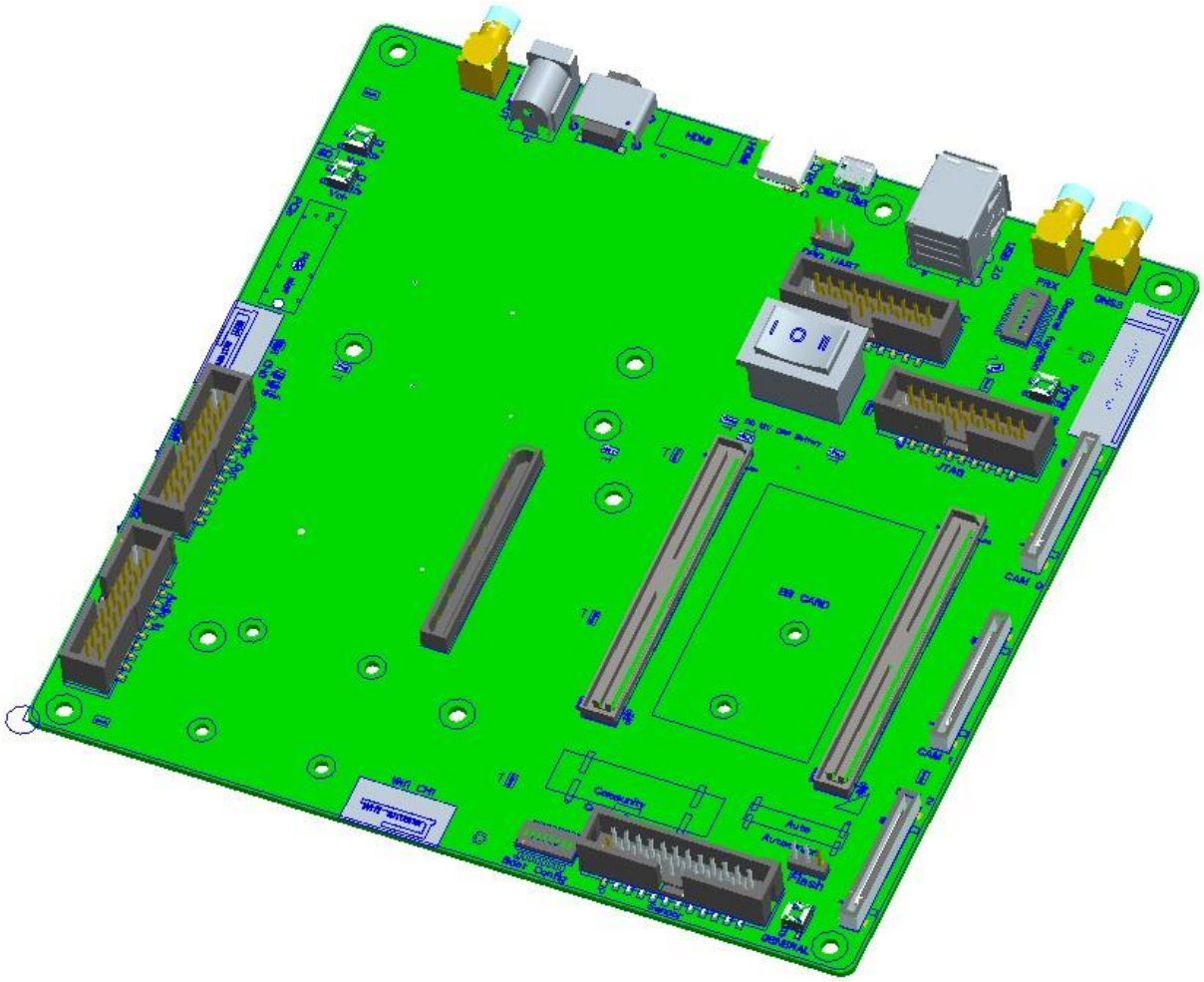

Figure 6 Open- Q™ 660 Carrier Board

3.8.1 Dip switch S10 Configuration Options

There is a DIP switch S2301 on the south top side of the Open-Q 660 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of this DIP switches.

Table 3.8-2 Dip Switch S2301 HW / SW configuration

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S2301-1	Toggles between FORCE USB boot and EDL mode. Enables FOCE USB (GPIO 57) when DIP switch turned on	Default out of the box configuration is OFF
WATCHDOG _DISABLE	S2301-2	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by SDA-GPIO 96	Default out of the box configuration is OFF
BOOT_CONFIG[1]	S2301-3	Enables SDA boot configuration 1 when DIP switch turned on. Controlled by SDA-GPIO 97	Default out of the box configuration is OFF
BOOT_CONFIG[2]	S2301-4	Enables SDA boot configuration 2 when DIP switch turned on. Controlled by SDA-GPIO98	Default out of the box configuration is OFF
BOOT_CONFIG[3]	S2301-5	Enables SDA boot configuration 3 when DIP switch turned on. Controlled by SDA GPIO60 See schematic for boot configuration options. Carrier board	Default out of the box configuration is OFF
N/C	S2301-6	NA	NA
N/C	S2301-7	NA	NA
N/C	S2301-8	NA	NA

There is another DIP switch S2302 on the north top side of Open-Q 660 carrier board. The 8-bit switch allows the user to control the system configuration and boot options.

Table 3.8-3 Dip Switch S2302 HW / SW configuration

Function	DIP Switch	Description	Notes
CHARGE_DISABLE	S2302-1	Disable charge when DIP switch turned on	Default out of the box configuration is OFF which enables system charge from USB **Note:** make sure turn on this switch when DC-12V input and USB are both present
N/C	S2302-2	NA	NA
HUB_RESET_SW	S2302-3	Enables hardware reset from general switch(J2204) when DIP switch turned on	Default out of the box configuration is OFF **Note:** Default HUB reset control is from s/w, hardware rework is needed to enable this function
MSM_PS_HOLD	S2302-4	Enables the JTAG_PS_HOLD mode when DIP switch turned on	Default out of the box configuration is OFF
N/C	S2302-5	NA	NA
N/C	S2302-6	NA	NA
N/C	S2302-7	NA	NA
BLSP_TP_CONFIG	S2302-8	Config the signals connected to BLSP_TP	Default out of the box configuration is OFF **Note:** SSC SPI2 is routed to BLSP_TP by default

Warning! : Before making any changes to the dip switch, make sure to note down the previous configuration. The default switch settings are above.

3.8.2 Carrier Board Expansion Connectors

The following table lists the connectors, expansions and their usages on the carrier board:

Table 3.8-4 Carrier Board Expansion Options and Usage

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	Battery connector	8 pin header	For providing power from 4.35V/3000mAh battery
Debug Serial via USB	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
JTAG	OS / Firmware /QFROM Programming / Debugging JTAG	Standard 20-pin connector, ARM and OpenDSP – Lauterbach	QFROM / eMMC / Platform EEPROM programming ARM / Open DSP debugging
Buttons	Power	SMD Button	Power Button for Suspend / Resume and Power off
	Volume +	SMD Button	Volume +Key
	Volume –	SMD Button	Volume – Key
	General Purpose	SMD Button	Reserved button for general purpose
NFC Board Header	20 pin NFC expansion connectors	NA	NA
Micro SD	Micro SD card	4bit Micro SD card support	External Storage
ANC Audio Jack	Audio Jack Supported using WCD9335	ANC audio jack providing 2lineout and 1 headset drivers (shared with ANC)	Audio support
3-Digital Microphone via audio input expansion header	Audio expansion Supported using WCD9335	Digital Audio header	For Digital audio input for Digital MIC, I2S codec, Slim bus interface.
3-Analog Microphone via audio input expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For Analog audio input for Analog MIC (differential signal)
2-Loud Speaker via audio output expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For loud speaker output after signal has been processed
Earpiece via audio output expansion header	Audio expansion Supported using WCD9335	Analog Audio header	For earpiece output after signal has been processed
USB 2.0 Host	USB 2.0 Host	Type-A dual port header	For Mouse and Keyboard
USB 3.1	USB 3.1	Type-C header	Transfer data to and from CPU
WLAN Antenna	1X PCB Antenna	2.4 – 5 GHz	Antenna to Carrier board

GNSS Antenna	PCB Antenna	GNSS : 1574.42 MHz – 1576.42 MHz GLONASS : 1587 MHz – 1606 MHz COMPASS: 1559.05 to 1563.14MHz Galilei: 4.092MHz BW(centered on 1575.42MHz)	Antenna to Carrier board
LED	3xLED	Red : PMIC Driven Green: PMIC Driven Blue: PMIC Driven	Red : General purpose Green : General purpose Blue : General purpose
LCD Display and Touch connector	100 pin for LCD signals from B2B boards for display	4-lane MIPI DSI0 , DSI1 I2C/SPI/GPIO Backlight MIPI Alliance Specification v1.2 MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01, V1.2 MIPI C-PHY Specification v1.0	Can work as one dual DSI or both independent display
Sensor header	24 pin sensor header	24 pin sensor header	Header to connect sensor board.
SIM Card	WWAN SIM card connector (optional)	4bit Micro SIM card support	For WWAN mini PCI express cards (for internal use only – not supported)
CSI Camera connectors	3 x CSI port connector with CLK, GPIOS, CCI	Supports 3 x Camera interfaces via three separate connectors ▪ 3 x MIPI-CSI each 4 lane ▪ External flash driver control ▪ Support for 3D camera configuration ▪ Separate I2C / CCI control MIPI Alliance Specification v1.2 for Camera Serial Interface	See Note: 36

The sections below will provide in depth information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 660 Processor board. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

3.8.2.1 Power Options

The Open-Q 660 Hardware Development Kit power source connects to the 12V DC power supply jack J0701. Starting from the power jack, the 12V power supply branches off into

different voltage rails via step down converters on the carrier board and PMIC on the Processor board. The Processor board is powered by 3.8V via a Silergy step down converter U0703 on the carrier board. To ensure the Processor board is getting powered correctly, user can monitor the current going into the Processor board via the power probe header J0901 (see section below).

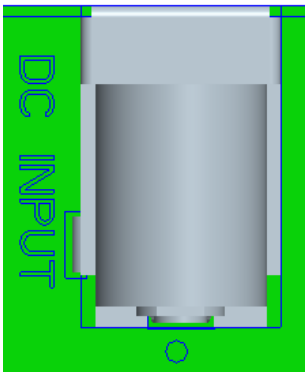

Figure 7 J0701 12V DC Power Jack

The Processor board has 2 PMIC modules. Functionalities of the 2 modules are outlined below.

PM660 PMIC is used for:

- Source various regulated power rails
- Support for battery charging on the PM660 is configurable on the platform. The carrier board uses a 3.8V constant power input and battery to the Carrier board. A DIP switch is used to enable/disable charge function. Make sure turn off battery charging when 12V DC in is used and USB charger is inserted.
- Source system clock

PM660A PMIC is used for:

- Source various regulated power rails

3.8.2.2 Debug Serial UART header J2103

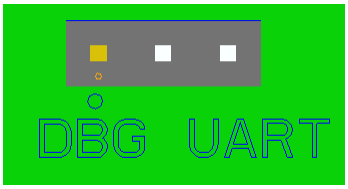

Figure 8 J2103 3.3V TTL Debug UART

The UART header and supporting circuitry does not come preinstalled. To have access to the debug UART, a 3-pin header needs to be installed as well as the supporting circuitry. Please see the carrier board schematic for details on what to install for this header to be functional.

The header consists of TX, RX and GND pins. It is a 3.3V TTL UART header. To get the serial terminal working with a PC, the following cable (or similar) is needed

http://www.digikey.ca/product-detail/en/TTL-232R-RPI/768-1204-ND/4382044

Table 3.8-5 Debug UART Header J2103 Pin-out

Description	Signal	pin	FTDI RPI cable connection
SDA UART RX (GPIO5)	BLSP2_UART_RX	J2103[1]	Orange
SDA UART TX (GPIO4)	BLSP2_UART_TX	J2103[2]	Yellow
GND	GND	J2103[3]	Black

3.8.2.3 Debug Serial UART over USB J2102

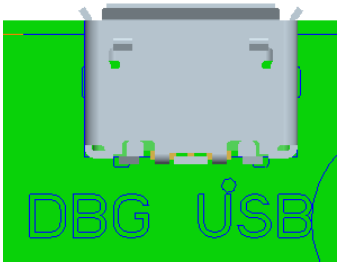

Figure 9 J2102 Debug UART over USB

The UART connection used on the HDK660 is a USB micro B connector (J2102). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

3.8.2.4 JTAG header J2101

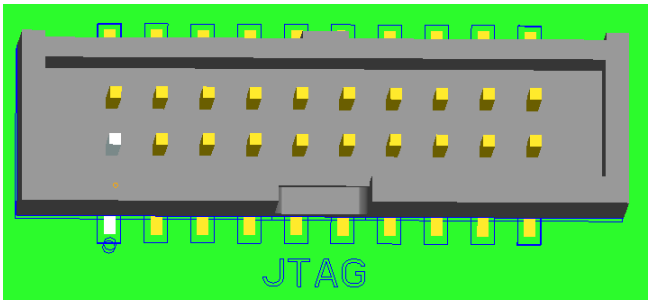

Figure 10 J2101 JTAG header

This connector provides a JTAG interface to the main processor by which users can connect a JTAG (Lauterbach / USB Wiggler) 20 pin ARM JTAG.

NOTE: The development kit does not include software support for JTAG

Table 3.8-6 JTAG Header J2101 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
GND	GND	J2101[2]	JTAG Power detect	JTAG_PWR	J2101[1]
GND	GND	J2101[4]	Target RESET_N signal	TRST_N	J2101[3]
GND	GND	J2101[6]	TDI Signal (Target DATA IN)	TDI	J2101[5]
GND	GND	J2101[8]	TMS Signal	TMS	J2101[7]
GND	GND	J2101[10]	TCK Signal	TCK	J2101[9]
GND	GND	J2101[12]	JTAG_RTCK signal	JTAG_RTCK	J2101[11]
GND	GND	J2101[14]	TDO Signal (Target Data Out)	TDO	J2101[13]
GND via 4.7KΩ pull down	GND	J2101[16]	Source RESET_N signal	SRST_N	J2101[15]
GND	GND	J2101[18]	NC	NC	J2101[17]
JTAG detect N signal	DET_N	J2101[20]	GND via 4.7KΩ pull down	GND	J2101[19]

3.8.2.5 Sensor IO Expansion Header J2501

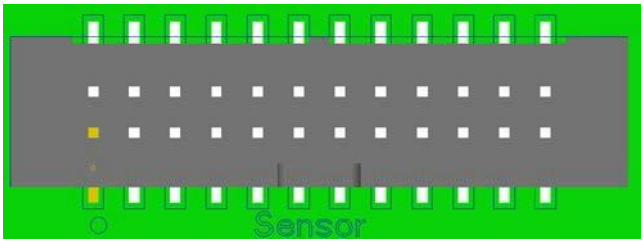

Figure 11 J2501 SENSOR EXPANSION HEADER

The sensor expansion header J2501 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin breakout for sensor expansion header J2501

Table 3.8-7 Sensor Expansion Header J2501 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
SSC I2C-3 serial data	SSC_I2C_3_SDA	J2501[1]	Accelerometer interrupt input to processor via GPIO68	ACCEL_INT_N	J2501[2]
SSC I2C-3 serial clock	SSC_I2C_3_SCL	J2501[3]	Cap interrupt input to processor via GPIO74	CAP_INT_N	J2501[4]
Sensor reset signal from processor to sensor via GPIO42	MEMS_RESET_N	J2501[5]	Gyroscope interrupt input to processor via GPIO69	GYRO_INT	J2501[6]
Sensor IO PWR 1.8 V VREG_LVS2A_1P8 power supply regulator (Digital)	SENS_IO_PWR	J2501[7]	Sensor Analog power supply from VREG_L19A 2.85V or 3.3V	SENS_ANA_PWR	J2501[8]
GND	GND	J2501[9]	GND	GND	J2501[10]
HRM interrupt/ configurable GPIO73	HRM_INT	J2501[11]	Touch screen interrupt input from processor via GPIO67	TS_INT	J2501[12]
SSC SPI-1 chip select 2	SSC_SPI_1_CS1_N	J2501[13]	Alternate sensor interrupt input to processor via GPIO71	ALSPG_INT_N	J2501[14]
MISC GPIO for sensor via GPIO11	SDA_GPIO11	J2501[15]	Digital Compass interrupt input to processor via GPIO70	MAG_DRDY_INT	J2501[16]
NC	NC	J2501[17]	Hall sensor interrupt input to processor via GPIO75	HALL_INT_N	J2501[18]
SSC SPI-1 chip select 1	SSC_SPI_1_CS_N	J2501[19]	SSC SPI-1 data master out/ slave in	SSC_SPI_1_MOSI	J2501[20]
SSC SPI-1 clock	SSC_SPI_1_CLK	J2501[21]	SSC SPI-1 data master in/ slave out	SSC_SPI_1_MISO	J2501[22]
NC	NC	J2501[23]	SSC power enable	SSC_PWR_EN	J2501[24]

In summary, if sensor application is not needed, this expansion header can provide SSC SPI1 and I2C. Please refer to the schematic and consider the power before connecting anything to this header.

3.8.2.6 NFC Expansion Header J2401

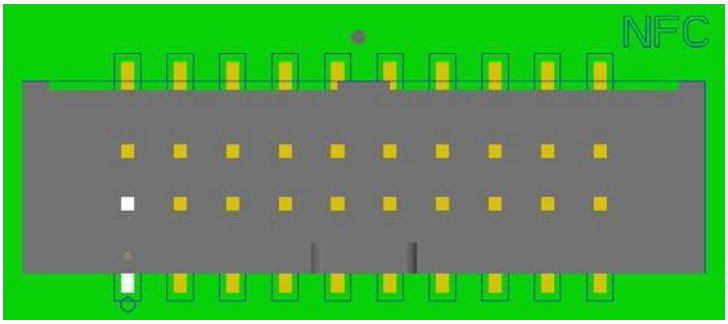

Figure 12 J2401 NFC EXPANSION HEADER

The NFC expansion header provides a 20 pin connector for attaching an optional NFC board This header also allows user to connect to the free GPIOs and I2C lines when NFC is not used; therefore, enabling other use cases. Please refer to Table below for detailed information regarding the signals that are being brought out by this connector.

Table 3.8-8 NFC Expansion Header J2401 pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
BLSP1 bit 0 via SDA GPIO3	NFC\SPI_CLK	J2401[1]	BLSP1 bit 2 via SDA GPIO1	NFC_SPI_MISO	J2401[2]
NFC power requestvia GPIO31	NFC_ESE_PWR_REQ	J2401[3]	SIM present GPIO via SDA GPIO90	UMI1_DET_N	J2401[4]
SIM Card DATA line (UIM1) via SDA GPIO87	UIM1_DATA	J2401[5]	150mA max 3.8V carrier board power supply	VPH_PWR	J2401[6]
SIM Card Reset line (UIM1) via SDA GPIO89	UIM1_RESET	J2401[7]	NFC interrupt IRQ pin via SDA GPIO28	NFC_INT_REQ	J2401[8]
SIM CLK line (SIM1) via SDA GPIO88	UIM1_CLK	J2401[9]	NFC Disable signal via SDA GPIO29	NFC_ENABLE	J2401[10]
1.8V Voltage regulator supply max 150mA via PM660	VREG_L9A_1P8	J2401[11]	BLSP8 I2C Bus-8 I2C SDA line	NFC_I2C6_SDA	J2401[12]
1.8V Voltage regulator supply max 150mA via PM660	VREG_S4A_1P8	J2401[13]	BLSP68I2C Bus-8 I2C CLK line	NFC_I2C6_SCL	J2401[14]
GND	GND	J2401[15]	NFC clock request signal via PM GPIO4	NFC_LNBBCLK3_EN	J2401[16]
PM660 free running clock via buffer	LNBB_CLK3_NFC	J2401[17]	NFC download request via SDA GPIO30	NFC_DWL_REQ	J2401[18]
BLSP1 1 bit via SDA GPIO2	NFC_SPI_CS_N	J2401[19]	BLSP1 3 bit via SDA GPIO0	NFC_SPI_MOSI	J2401[20]

In general, if there is no need for NFC application, this expansion header can provide two GPIOs, I2C, free running clocks, and enable voltage/ power source to external peripherals.

3.8.2.7 ANC Headset Jack J1501

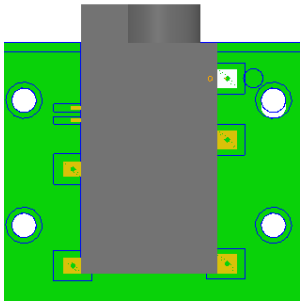

Figure 13 ANC HEADPHONE JACK

The ANC headset jack (J1501) is a special 3.5mm TRRS jack with ANC capabilities. It is backwards compatible with standard headset jacks.

3.8.2.8 Audio Inputs Expansion Header J1601

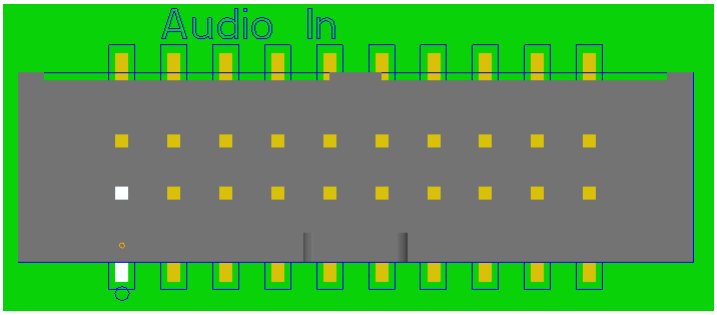

Figure 14 J1601 Audio Inputs Expansion Header

This header expansion provides the following audio inputs:

- 3 digital mics
- 3 analog mics
- Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio inputs expansion header J1601:

Table 3.8-9 Audio Inputs Expansion Header J1601 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_IN1_P	J1601[1]	Analog MIC1 negative differential input	CDC_IN1_N	J1601[2]
Analog MIC2 positive differential input	CDC_IN5_P	J1601[3]	Analog MIC2negative differential input	CDC_IN5_N	J1601[4]
MIC bias output voltage 1	MIC_BIAS1	J1601[5]	MIC bias output voltage 3	MIC_BIAS3	J1601[6]
Analog MIC3 positive differential input	CDC_IN6_P	J1601[7]	Analog MIC3 negative differential input	CDC_IN6_N	J1601[8]
MIC bias output voltage 4	MIC_BIAS4	J1601[9]	3.3V power supply max 500mA	MB_VREG_3P3	J1601[10]
GND	GND	J1601[11]	GND	GND	J1601[12]
Clock for digital MIC3	CDC_DMIC_CLK1	J1601[13]	Clock for digital MIC1	CDC_DMIC_CLK2	J1601[14]
Digital MIC3data line	CDC_DMIC_DATA1	J1601[15]	Digital MIC1data line	CDC_DMIC_DATA2	J1601[16]
1.8V power supply max 300mA	VREG_S4A_1P8	J1601[17]	Clock for digital MIC2	CDC_DMIC_CLK3	J1601[18]
GND	GND	J1601[19]	Digital MIC2data line	CDC_DMIC_DATA3	J1601[20]

3.8.2.9 Audio Outputs Expansion Header J1602

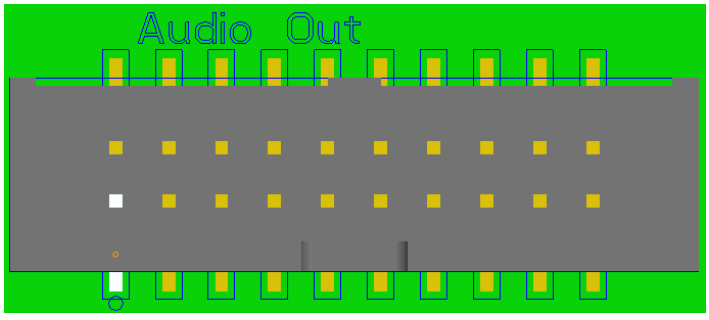

Figure 15 J1602 Audio Outputs Expansion Header

This header expansion provides the following audio outputs:

- 2 differential analog audio line out
- 2 single ended analog audio line out
- 1 differential analog earpiece amplifier output (no external amp needed)
- 2 speaker amplifier enable control

- Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J1602:

Table 3.8-10 Audio Inputs Expansion Header J1601 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out 1, positive differential output	LINE_OUT1_P	J1602[1]	Analog audio line out 1, negative differential output	LINE_OUT1_N	J1602[2]
Analog audio line out 2, positive differential output	LINE_OUT2_P	J1602[3]	Analog audio line out 2, negative differential output	LINE_OUT2_N	J1602[4]
Audio line single end outputs GND reference(connect to ground)	LINE_REF	J1602[5]	3.3V output power supply	MB_VREG_3P3	J1602[6]
Analog audio line out 1, single ended output	LINE_OUT3	J1602[7]	Analog audio line out 2, single ended output	LINE_OUT4	J1602[8]
Analog earpiece amplifier out, positive differential output	CDC_EAR_P	J1602[9]	Analog earpiece amplifier out, negative differential output	CDC_EAR_M	J1602[10]
GND	GND	J1602[11]	3.8V output power supply	VPH_PWR	J1602[12]
Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_CLK	J1602[13]	Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_DATA	J1602[14]
Speaker amplifier enable 1	WSA_EN	J1602[15]	Speaker amplifier enable 2	SPKR_AMP_EN2(DNI)	J1602[16]
1.8V output power supply	VREG_S4A_1P8	J1602[17]	12V output power supply	DC_IN_12V	J1602[18]
5.0V output power supply	MB_VREG_5P0	J1602[19]	GND	GND	J1602[20]

3.8.2.10 USB TYPE A Connector J1101

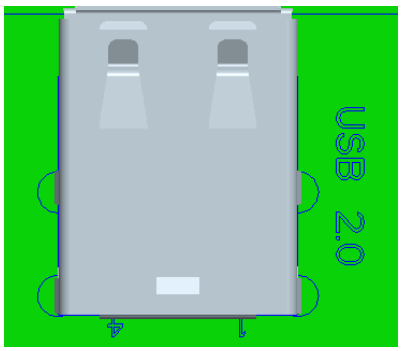

Figure 16 J1101 USB2.0 Type A Connector

The on-board USB type A connector supports 2x USB 2.0 host interface.

3.8.2.11 USB3.1 Type-C Connector J1201

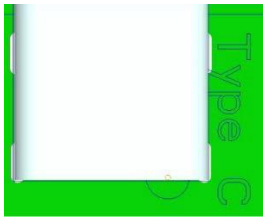

Figure 17 J1201 USB3.1 Type-C Connector

The on-board Type-C connector supports USB 3.1 Gen1, which also supports Type-C with DisplayPort V1.3.

Visit http://support.intrinsyc.com for a list of suggested HDMI and Display port dongles

3.8.2.12 On Board PCB WLAN Antenna

The HDK660 carrier board has two on-board PCB antennas that connects to the WCN3980 WiFi module on the carrier board via coaxial cables that attaches to MH4L receptacles. These antennas connect to the carrier board in the following configuration:

- WLAN0 on the carrier board connects to ANT0 on the WCN3980 WiFi module

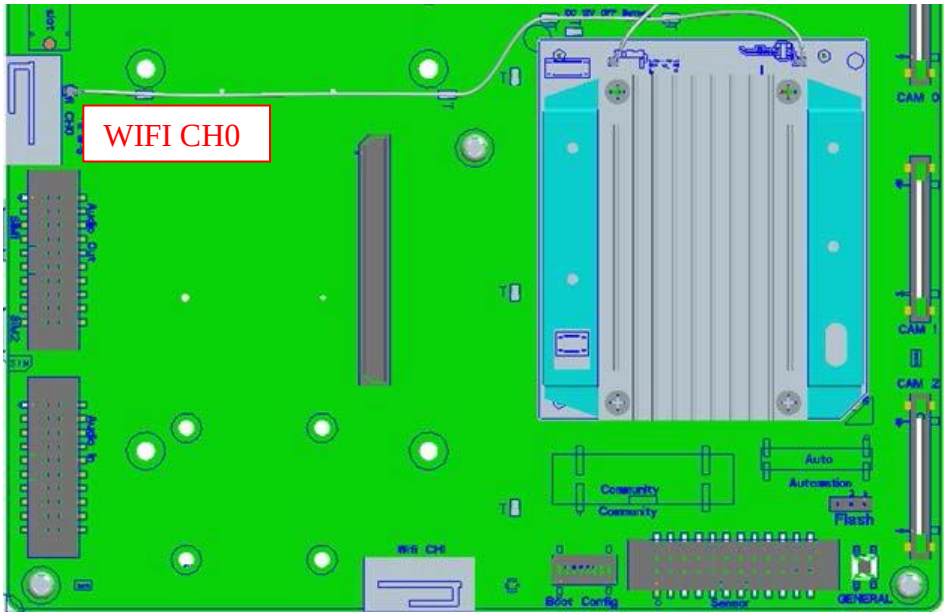

Figure 18 On Board PCB WLAN Antennas

3.8.2.13 On Board PCB GNSS Antenna

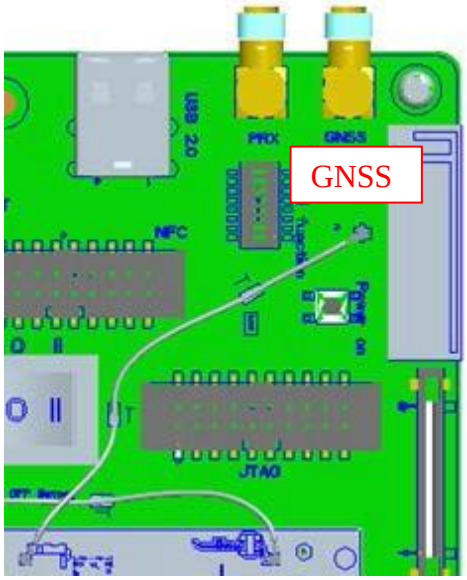

Figure 19 GNSS On Board PCB GNSS Antennas

The HDK660 carrier board has one on-board PCB antennas on the bottom side that connects to the Carrier board via coaxial cable that attaches to MH4L receptacles. The on-board antenna is connected to the Carrier board by default, meanwhile, there are 0ohm jumpers for user to use an external GNSS antenna via the SMA connector. The option pads are between the antenna and the eLNA input.

Table 3.8-11 GNSS Antenna Option

Option	R3804	R3805
On-Board	DNI	Stuff
SMA connector	Stuff	DNI

3.8.2.14 GNSS SMA Connector J3802

The GNSS SMA connector is reserved for user to use an external antenna. Refer to Table 3.8-11, stuff R3804 and remove R3805 to make the path active.

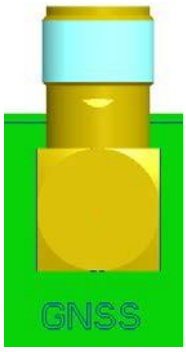

Figure 20 GNSS SMA Connector

3.8.2.15 Camera connectors

The HDK660 development kit supports three 4-lane MIPI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals
- Reserved J1702 for integrated flash driver
- Support for 3D camera configuration
  - Separate I2C control (CCI0, CCI1)
- Supports all CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-VF connector to access signals such as MIPI, CLK, GPIO and power rails

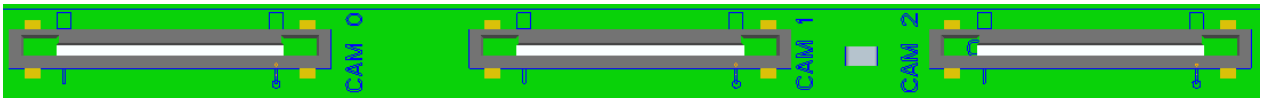

Figure 21 Camera Connectors (J1701, J1801, J1901)

Figure 21 above shows the three MIPI CAM0 (J1701), CAM1 (J1801) and CAM2 (J1901) connectors. The table below outlines the pin outs of these connectors

Table 3.8-12 MIPI CSI Camera Connector Pinouts (J1701, J1801, J1901)

Pin#	CAM0(J1701)	CAM1(J1801)	CAM2(J1901)	Description
1	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
2	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
3	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
4	GND	GND	GND	Ground
5	MB_ELDO_CAM0_AVDD	MB_ELDO_CAM1_AVDD	MB_ELDO_CAM2_AVDD	Power output. Connected to external LDO output. Default MB_ELDO_CAM0_AVDD is 1.8V(DNI R0843 and solder R0844 to set this power rail as +2.8V), MB_ELDO_CAM1_AVDD and MB_ELDO_CAM2_AVDD are +2.8V. Maximum current 300mA
6	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to external LDO regulator. Default value is set to 1.05/1.1/1.2V according to sensor spec . Maximum current 500mA
7	MB_ELDO_CAM0_VCM	MB_ELDO_CAM1_VCM	MB_ELDO_CAM2_VCM	Power output. Connected to external LDO. Default is +2.8V. Maximum current 300mA
8	MB_ELDO_CAM0_VCM	MB_ELDO_CAM1_VCM	MB_ELDO_CAM2_VCM	Power output. Connected to external LDO. Default is +2.8V. Maximum current 300mA
9	VREG_LVS1A_1P8	VREG_LVS1A_1P8	VREG_LVS1A_1P8	Power output. Connected to PM660 VREG_L11A switch output. Default is +1.8V. Maximum current 300mA
10	VREG_LVS1A_1P8	VREG_LVS1A_1P8	VREG_LVS1A_1P8	Power output. Connected to PM660 VREG_L11A switch output. Default is +1.8V. Maximum current 300mA
11	GND	GND	GND	Ground
12	FLASH_STROBE_EN (SDA_GPIO40)	FLASH_STROBE_EN (SDA_GPIO40)	FLASH_STROBE_EN (SDA_GPIO40)	Output. Connected to SDA660 Default use is for camera flash strobe enable
13	CAM0_RST_N (SDA_GPIO46)	CAM2_RST_N (SDA_GPIO48)	CAM1_RST_N (SDA_GPIO47)	Output. Connected to SDA660 GPIO46 / GPIO47 / GPIO48. Default use is for camera reset
14	CAM0_STANDBY_N (SDA_GPIO44)	CAM2_STANDBY_N (SDA_GPIO51)	CAM1_STANDBY_N (SDA_GPIO50)	Output. Connected to SDA660 GPIO44 / GPIO50 / GPIO51. Default use is for camera standby
15	CCI_I2C_SCL0 (SDA_GPIO37)	CCI_I2C_SCL0 (SDA_GPIO37)	CCI_I2C_SCL0 (SDA_GPIO37)	Output. Connected to SDA660 GPIO37. Default use is for camera CCI0 I2C clock interface
16	CCI_I2C_SDA0 (SDA_GPIO36)	CCI_I2C_SDA0 (SDA_GPIO36)	CCI_I2C_SDA0 (SDA_GPIO36)	Input / output. Connected to SDA660 GPIO36. Default use is for camera CCI0 I2C data interface
17	CAM_MCLK0_BUF (SDA_GPIO32)	CAM_MCLK2_BUF (SDA_GPIO34)	CAM_MCLK1_BUF (SDA_GPIO33)	Output. Connected to SDA660 GPIO32 / GPIO33 / GPIO34. Default use is for camera master clock. Maximum 24MHz

Pin#	CAM0(J1701)	CAM1(J1801)	CAM2(J1901)	Description
18	FLASH_STROBE_TRIG (SDA_GPIO41)	FLASH_STROBE_TRIG (SDA_GPIO41)	FLASH_STROBE_TRIG (SDA_GPIO41)	Output. Connected to SDA660 GPIO41. Default use is for camera flash strobe trigger
19	GND	GND	GND	Ground
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	MIPI_CSI2_LANE0_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	MIPI_CSI2_LANE0_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
22	GND	GND	GND	Ground
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI2_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI2_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
25	GND	GND	GND	Ground
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	MIPI_CSI2_LANE1_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	MIPI_CSI2_LANE1_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
28	GND	GND	GND	Ground
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	MIPI_CSI2_LANE2_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	MIPI_CSI2_LANE2_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
31	GND	GND	GND	Ground
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	MIPI_CSI2_LANE3_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	MIPI_CSI2_LANE3_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
34	GND	GND	GND	Ground
35	CCI_I2C_SDA1 (SDA_GPIO38)	CCI_I2C_SDA1 (SDA_GPIO38)	CCI_I2C_SDA1 (SDA_GPIO38)	Output / Input. Connected to SDA660 GPIO38. Default use is for camera CCI1 I2C data interface
36	CCI_I2C_SCL1 (SDA_GPIO39)	CCI_I2C_SCL1 (SDA_GPIO39)	CCI_I2C_SCL1 (SDA_GPIO39)	Output. Connected to SDA660 GPIO39. Default use is for camera CCI1 I2C clock interface
37	CAM_IRQ (SDA_GPIO43)	CAM_IRQ (SDA_GPIO43)	CAM_IRQ (SDA_GPIO43)	Input. Connected to SDA660 GPIO43. CAM_IRQ signal
38	CAM0_MCLK3 (SDA_GPIO35)	CAM1_MCLK3 (SDA_GPIO35)	CAM2_MCLK3 (SDA_GPIO35)	Output. Connected to SDA660 GPIO35. Default use is for camera master clock. Maximum 24MHz
39	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to external LDO regulator. Default is +1.2V. Maximum current 500mA
40	MB_VREG_5P0	MB_VREG_5P0	MB_VREG_5P0	Power output. 5V Power supply. Maximum 700mA
41	MB_VREG_5P0	MB_VREG_5P0	MB_VREG_5P0	Power output. 5V Power supply. Maximum 700mA

A connection from the camera connectors on the carrier board to the camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

The table below shows the combinations of camera usage for different use cases.

Table 3.8-13 MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or 2 x Camera of 1 lane each
CSI0 + CSI1	Up to 4 lane 3D	4 lane 3D use case / Dual 4 lane configuration
CSI 2	Up to 1 lane 3D	1 lane 3D use case / Dual 1 lane configuration
CSI0 + CSI1 + CSI2	Up to 4 lane	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0

3.9 Display Card

Table 3.9-1 Display Card Mechanical Properties

Dimension	61.48cm^2 (106mm x 58 mm)
Major Interfaces	one 100-pin high speed board-to-board connector

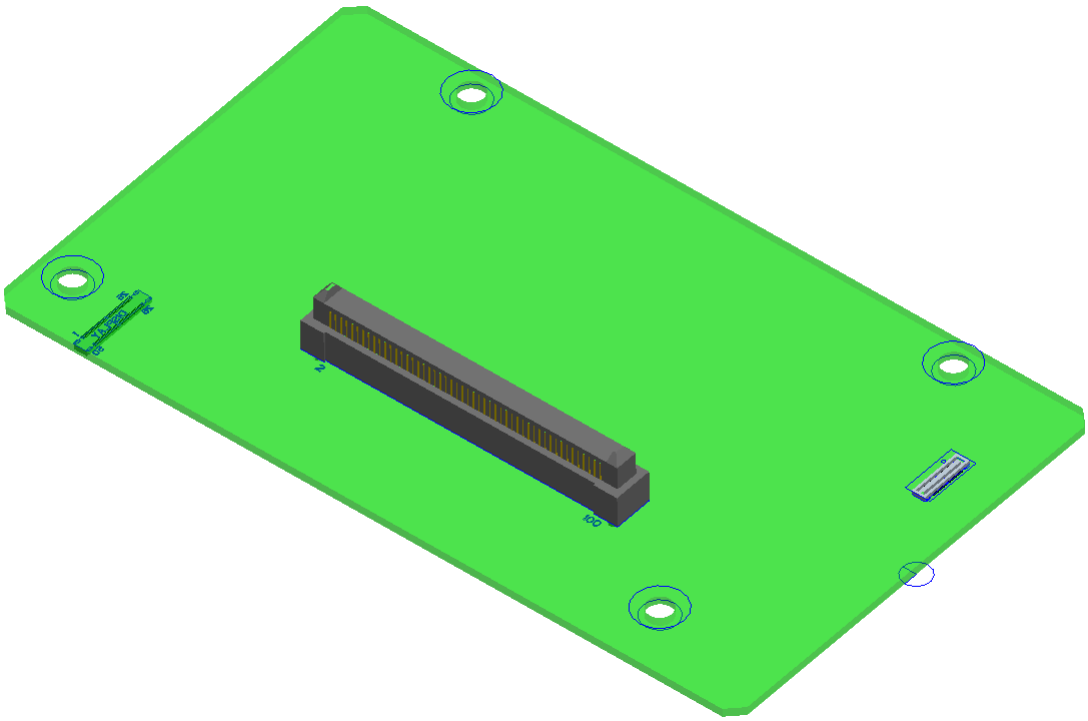

Figure 22 HDK 660 Display Card

3.9.1 Display Card Overview

The display output options for the HDK660 Development Kit consists of A 100-pin display connector J0501 that supports:

- Dual DSI DPHY 1.2
- Touch screen capacitive panels via I2C, SPI, and interrupts (up to two devices)
- Backlight LED
  - Can support external backlight driver control and power
  - PM660A Triple supply topology for AMOLED display panels

The development platform can support the following display combinations

MIPI DSI	1 x 4lane DSI0 + 1 x 4lane DSI1 2 x 4-lane DSI DPHY 1.2 Support up to WQXGA (2560 x 1600) at 60fps

3.9.2 Display Card Connector J0501

The 100-pin display card connector provides the following features/ pin-outs that enables the development kit to connect to a MIPI DSI panel/ device:

NOTE: Please refer to the carrier schematic and display card tech notes when designing a custom display card.

- DSI
  - 2 x 4 lane DSI
- Backlight
  - Dual synchronous SMPS topology: boost (LAB module) and inverting buckboost (IBB module) and gamma bias (OLEDB) module
    - Input voltage range: 2.8 V to 4.75 V
    - LAB: +4.6 V to +5 V programmable; default is +4.6 V
    - IBB: -0.8 V to -5.4 V programmable; default is -4 V
    - OLEDB: +5.8 V to +7.9 V programmable
- Display connector
  - AMOLED with integrated backlight
  - TFT with external backlight
- Additional GPIOs for general purposes available
- VREG_L13A voltage rail from PM660
  - Required by display for DOVDD
  - 300mA current path
- Touch Panel
  - Supports up to two touch screen controllers
  - Supports I2C or SPI via BLSP4 and SSC_SPI_2
  - Can chose between I2C or SPI signals via

MUX Power specifications:

The display card connector supports the following power domains:

Table 3.9-2 Display Power Domains

Display Signal	Power Domain
PM660 VREG_OLEDB (5.8V~7.9V with SWIRE control)	up to 60 mA
PM660 VREG_L6B (3.3V)	up to 50 mA
PM660 VREG_L11A (1.8V)	up to 150 mA
PM660 VREG_L13A (1.8V)	up to 600 mA
Carrier 3.3V	up to 0.5A
Carrier 5 V	up to 1.5A
Carrier 12 V	up to 0.5A

HDK660 display card (part number: 20-PB892-H10) is an additional PCBA that mates with the display connector J1301 on the carrier board. This board allows users to interface with the development kit via the LCD (see below for details) that comes preinstalled on the display card. Figure 23 illustrates the interfacing connectors on the display card.

The display card comes as an additional add-on to the HDK660 development kit.

3.9.2.1 Connecting the Display Card to the Development Kit

This configuration allows the user to use the preinstalled LCD display that comes with the display board. As shown in the block diagram below, the MIPI DSI0 lines, which come from the 100-pin ERM8 connector, directly connects to the FHD AMOLED panel. See the section below for more details on this LCD panel. It is important to note that connector J0501 of the display card needs to connect to J1301 of the carrier board for this configuration to work.

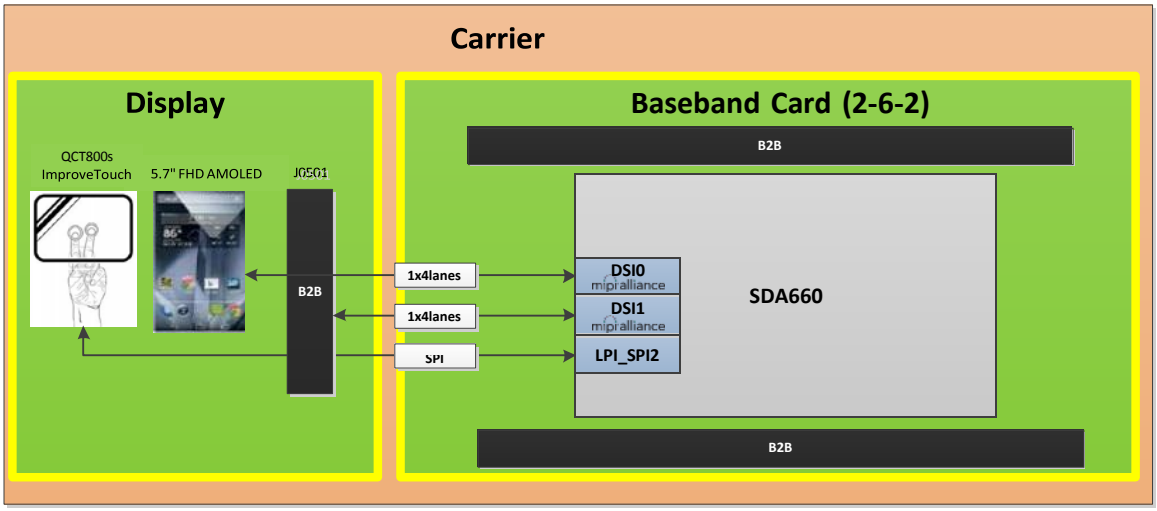

Figure 23 Display Card Default Configuration

3.9.3 Display panel

This LCD panel comes preinstalled on the HDK660 display card. Below are the Panel specifications:

- Resolution: 1920x1080
- LCD Type: AMOLED
- PCAP touch panel
- No of Lanes: 1 x 4 lane MIPI DSI interface via Display Card.
- Diagonal Length: 5.7”