Open-X™ 8M Development Kit based on the NXP i.MX8™ Processor

User Guide

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IDENTIFICATION

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1. INTRODUCTION

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-X™ 8M Development Kit based on the NXP i.MX8™ Processor

For more background information on this development kit, visit: https://www.intrinsyc.com/imx-embedded-development-kits/open-x-8m-development-kit/

1.2 Scope

This document will cover the following items on the Open-X 8M:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Display Board for LCD (Optional)

1.3 Intended Audience

This document is intended for hardware or software developers who would like to design custom applications based on the Intrinsyc Open-X 8M Development Kit.

2. DOCUMENTS

This section lists the supplementary documents for the Open-X 8M development kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-X Development Kit

2.2 Reference Documents

REFERENCE	TITLE
R-1	Open-X 8M Schematics (SOM, Carrier)

2.3 Terms and Acronyms

Term and acronyms	Definition
B2B	Board to Board
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
HDMI	High Definition Media Interface
JTAG	Joint Test Action Group
MIPI	Mobile Industry processor interface
RF	Radio Frequency
SOM	System On Module
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed
PCIe	Peripheral Component Interconnect Express
NGFF	Next Generation Form Factor
I2C	Inter-Integrated Circuit

2.4 List of Figures

2.5 List of Tables

3. OPEN-X 8M DEVELOPMENT KIT

3.1 Introduction

The Open-X 8M provides a quick reference or evaluation platform for NXP Semiconductors latest processor series, the i.MX 8M. This kit is suited for Android or Linux application developers, multimedia audio or video vendors, voice processing vendors, consumer product manufacturers, OEMs, hardware component vendors, video surveillance, and camera vendors to evaluate, optimize, test and deploy applications that can utilize the NXP Semiconductors i.MX8 series technology.

3.2 Development Platform Notice

This development platform contains RF, analog and digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-X 8M Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-X 8M Development Kit includes the following:

- Open-X 8M SOM with the i.MX 8M processor
- Open-X 8M Development Board (Mini-ITX form-factor)
- Heatsink covering the SOM (not shown below)
- Open-Q™ LCD/touchpanel (Optional Accessory)
- AC power adapter and HDMI cable

Figure 3-1 Assembled Open-X 8M Development Kit

The development kit comes with Android software pre-programmed on the CPU board (SOM). Please contact Intrinsyc for availability of camera modules, sensor boards, and other accessories: sales@intrinsyc.com

3.5 Hardware Identification Label

Labels are present on the SOM and the carrier board. The following information is conveyed on these two boards:

SOM:

- Serial Number
- Wi-Fi MAC address
- Ethernet MAC address

Refer to http://support.intrinsyc.com/account/serialnumber for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: http://support.intrinsyc.com/account/register

Carrier board:

- Serial Number

Note: Please retain the SOM and carrier board serial number for warranty purposes.

3.6 System Block Diagram

The Open-X 8M development platform consists of three major components:

- Open-X 8M SOM
- Carrier board for I/O and connecting with external peripherals
- Display Adapter Board (optional accessory)

The following diagram explains the interconnectivity and peripherals on the development kit.

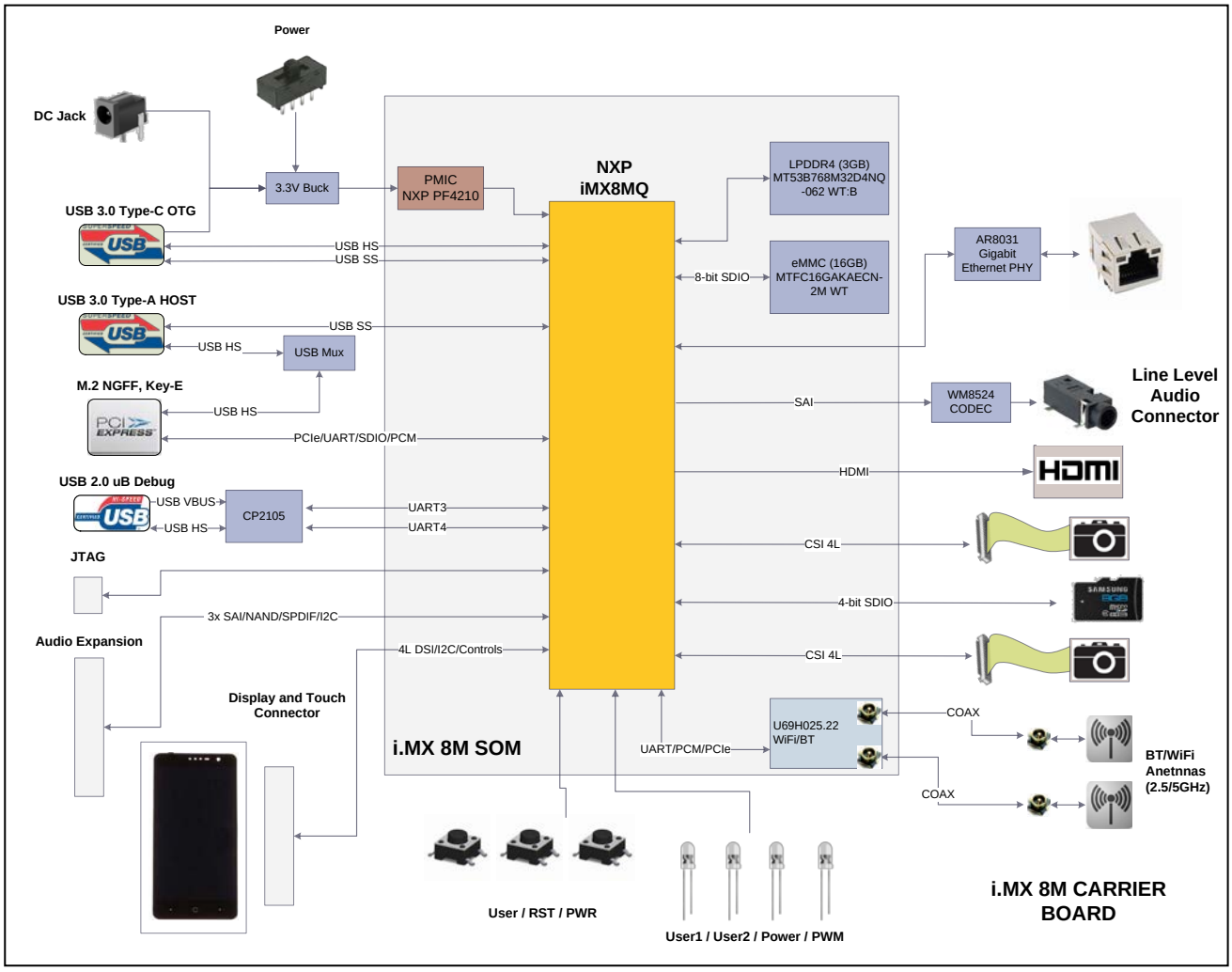

Figure 3-2 Open-X 8M Block Diagram

3.7 Open-X 8M SOM

The SOM provides the basic common set of features with minimal integration efforts for end users. It contains the following:

- i.MX 8M (MiMX8MQ6DVAJZAB) main application processor
- LPDDR4 1600MHz 3GB RAM
- 16 GB eMMC Flash storage
- MC34PF4210A1ES – PMIC for Peripheral LDOs, Boost Regulators
- QCA6174A-1 Wi-Fi + BT pre-certified module over PCIe, UART, PCM

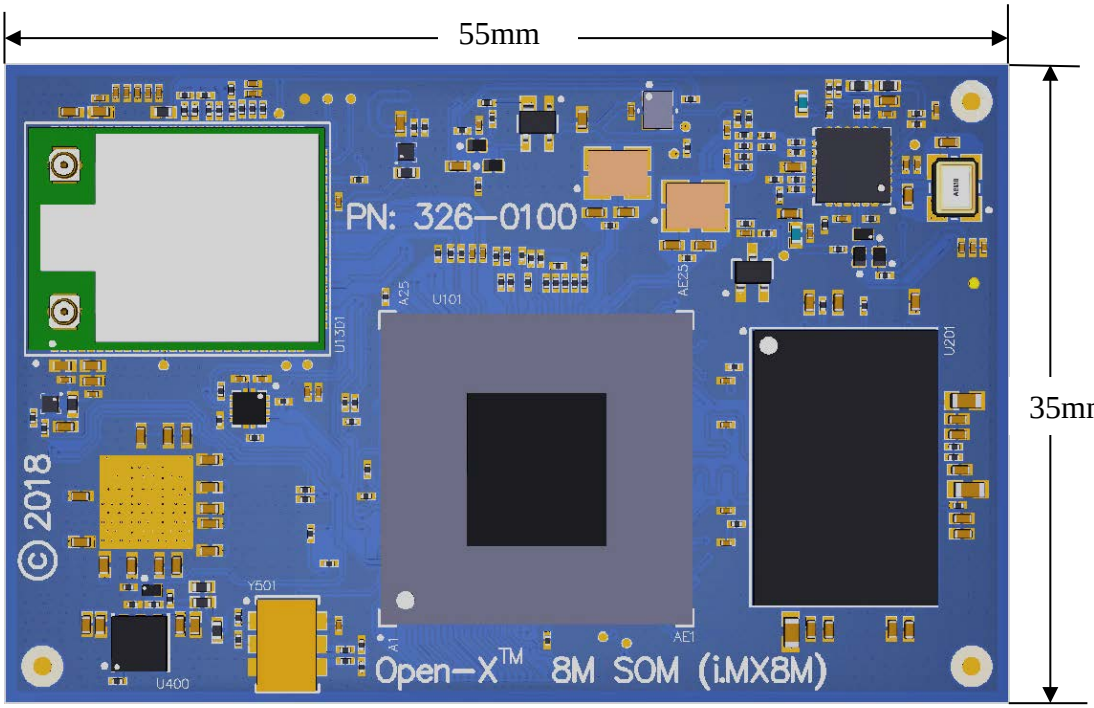

Figure 3-3 Open-X 8M SOM

3.7.1 SOM Mechanical Properties

Area	19.25 cm^2 (55 mm x 35 mm)
Interface	3x 100-pins SOM to carrier board connector (B2B Connector)
Thermal	An optional top side heat sink can be installed

3.7.2 SOM Block Diagram

The Open-X 8M SOM measuring 55mm x 35mm is where all the processing occurs. It is connected to the carrier via 3 100-pin B2B connectors.

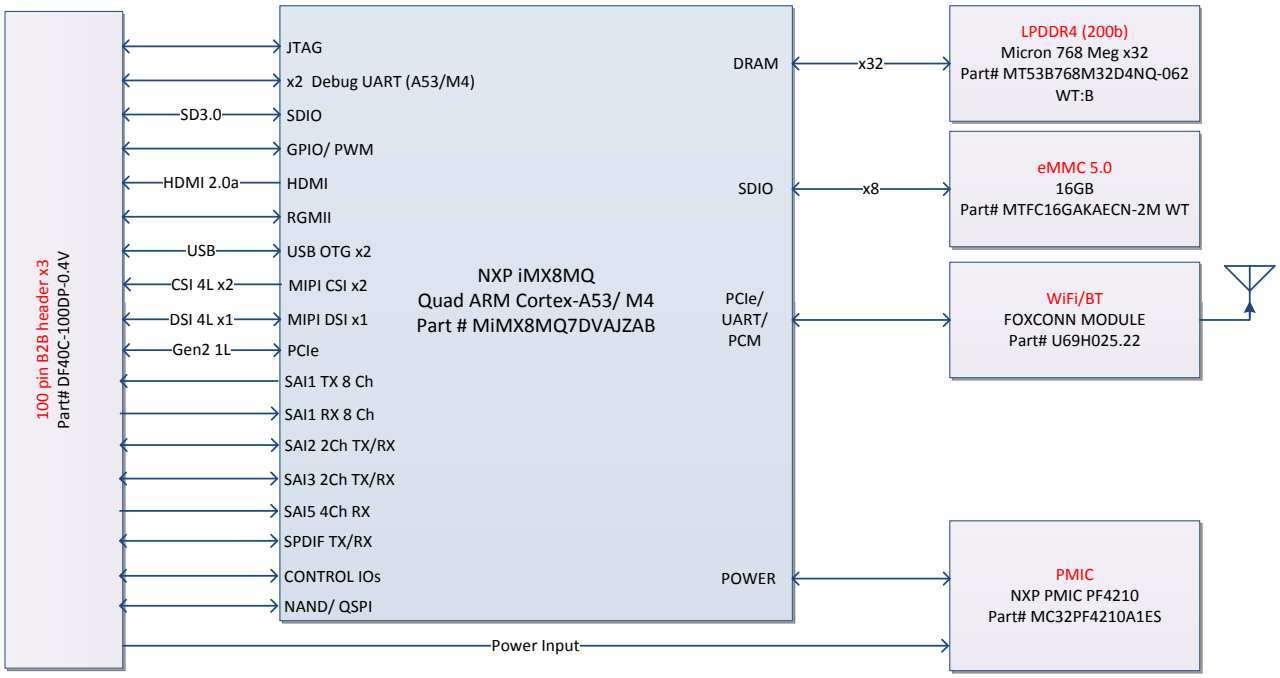

Figure 3-4 SOM Block Diagram

3.7.3 Hardware Specification

The Open-X 8M SOM platform encompasses the following hardware features:

Table 3.7.3-1 Open-X 8M SOM Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	MiMX8MQ6DVAJZAB	NXP's i.MX 8M family processor.	Quad ARM Cortex®-A53 and ARM Cortex®-M4 cores, 1.5GHz
	PMIC (PF4210)	NXP PMIC designed for i.MX 8M Processors	NA
Memory	3GB LPDDR4	Memory	Up to 1600MHz LPDDR4 Supported via 1x32bit DRAM channel
	16 GB eMMC	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	eMMC 5.0
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via QCA6174A-1 – PCIe	QCA6174A-1 Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac – 20/40 MHz at 2.4 GHz, 20/40/80 MHz at 5.0 GHz via QCA6174A-1 over PCIe1. Full 2x2 antenna configuration.
	BT V4.1 - 2.4 GHz via QCA6174A-1 – UART / PCM	QCA6174A-1 Wi-Fi + BT Combo Chip	Support BT 4.1 + HS, BLE and backward compatible with BT 1.x, 2.x + EDR
RF Interfaces	2xWLAN / BT MH4	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
Audio Interfaces	4 x SAI	Synchronous Audio Interface	SAI1 8ch TX/RX SAI2 2ch TX/RX SAI3 2ch TX/RX SAI5 4ch RX
	1 x SPDIF	Digital Audio Interface	SPDIF TX/RX

Interfaces	2 x MIPI CSI	Camera Connectors CSI1, CSI2	MIPI Alliance Specification v1.0
	2 x USB 2.0/ 3.0 OTG		USB3.0 Standard
	1 x MIPI DSI	100- pin display connector. Interfaces with Intrinsyc Display Adapter Board	MIPI Alliance Specification v1.01. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01
	2 x PCIe 1Lane Gen2		PCI Express Specification, Rev 2.1
	1 x Gigabit Ethernet	RGMII interface	
	1 x HDMI 2.0a	HDMI capable of 4K 60Hz content	HDMI 2.0a
	3 x Memory / Storage	1 x 8 bit NAND 1 x 4 bit QSPI 1 x 4 bit SDIO	JEDEC/MMC standard version 5.0, SD 3.0
	2 x I2C	I2C1, I2C3	
	2 x Debug UART	1x Enhanced UART for A53 1x Standard UART for M4	
	1 x JTAG		

3.7.4 SOM RF Specification for WIFI, BT

The SOM includes the following radio interfaces from a single QCA6174A-1 module:

- ANT1: Wi-Fi antenna 1 + BT
- ANT2: Wi-Fi antenna 2

Antenna 1: The antenna 1 connector is for one of the two Wi-Fi antennas as well as the single Bluetooth antenna.

Antenna 2: The antenna 2 connector is for the second Wi-Fi antenna.

By default, both antenna ports are connected by coaxial cables to the PCB trace antennas on the carrier board. Note that two dual-band (2.4GHz + 5GHz) antennas are required to be connected to achieve full performance of the Wi-Fi interface. If only Bluetooth is being used, then only a single 2.4GHz antenna connected to antenna 1 is necessary.

The SOM WiFi/BT module is a pre-certified module for FCC and Industry Canada (see FCC ID: 2AFDI-ITCNFA324 for details). Please note that the on-board PCB antennas were not the antennas used for the SOM WiFi/BT module certification.

For details on connecting the WiFi module to the on-board PCB antennas on the carrier board, refer to section below.

3.8 Open-X 8M Carrier Board

The Open-X 8M Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

Dimensions	289 cm^2 (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	SOM: 3x100 pin board to board connector Display: 100 pin carrier board connector

3.8.1 Boot dip switch Configuration Options

Two dip switches on the Open-X 8M carrier board provides the user options to configure the boot mode and boot device. The table below show the supported boot modes on the Open-X 8M Development Kit:

S701		
BOOT_MODE 1	**BOOT_MODE 0**	**BOOT SOURCE**
0	0	Fuses
0	1	Serial Downloader
1	0	Internal (see BOOT Device)
1	1	Reserved (do not use)

The table below shows the supported boot devices on the Open-X 8M Development Kit:

BOOT Device	**S700 [0:3]**
Boot from eMMC	0010
Boot from SD2	1100

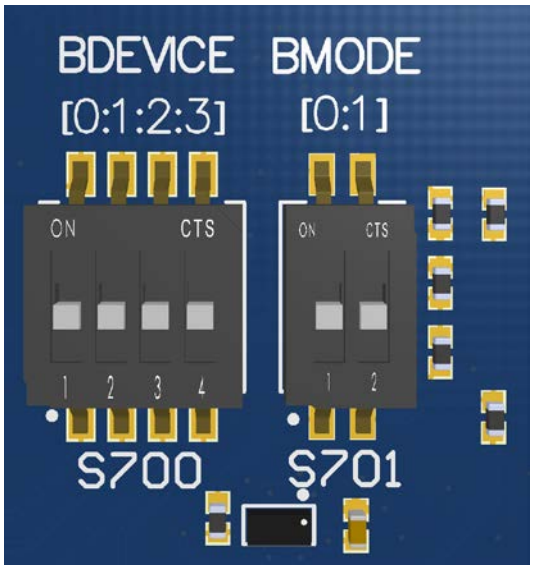

Figure 3-5 Boot Switches S700 and S701

3.8.2 Open-X 8M Carrier Board Expansion Connectors

Table 3.8.2-1 lists the connectors, expansions and their usages on the carrier board:

Table 3.8.2-1 Carrier Board Expansion options and their usage

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	USB Type-C	USB Type-C connector, 5V-20V, 100W	Power Supply or USB Type-C peripherals
Debug Serial via USB	Debug Serial UART console over USB for development	SILICON LABS CP2105 USB to UART for both A53 and M4 processors	Development Serial Connector for debug output via USB
JTAG	OS / Firmware Programming / Debugging JTAG	10-pin connector	eMMC / Platform programming ARM / OpenOCD debugging
Buttons	General Purpose SW button	SMD Button	Additional button for general purpose
	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
	Reset Button	SMD Button	Button for Reset
Micro SD (on bottom)	Micro SD card	4bit MicroSD SD3.0 card or MMC card support	External Storage
3.5mm Audio Jack	Audio Jack supported using CIRRUS LOGIC WM8524 audio codec	CTIA standard 3.5mm 4-pole audio jack providing 24bit 192kHz stereo line level audio	High quality stereo audio support
Audio Expansion	FPC connector for SAI lines	Supports SAI1, SAI3, SAI5, SPDIF as well as I2C3 and NAND	FPC connector for audio expansion boards
	3 x 0.05mm pitch headers for SAI lines	Supports SAI1, SAI3, SAI5, SPDIF as well as I2C3 and NAND	0.05mm headers for audio and GPIO expansion
RJ45 Gigabit Ethernet Connector	RJ45 jack with 2 bi-color LEDs	RJ45 with internal magnetics, supported using AR8031 Gigabit Ethernet PHY	For connecting to a wired LAN
HDMI Type-A Connector	Extended Display ports	HDMI port supports up to 4K without HDCP 2.0A spec	External Display
USB Type-C OTG	USB Type-C 3.0 OTG	Type-C connector	USB client / host port for Type-C peripherals or main power input
USB 3.0	USB 3.0	Type-A header	Host port for USB 3.0 peripherals
WLAN Antenna	2X PCB Antenna	2.4 – 5.1 GHz	Antenna to SOM WiFi module
LED	4xLED	Red : 12V provided and SW400 is on Green : CPU is running in overdrive mode Blue : General purpose Orange : General purpose	
LCD Display and Touch connector	100 pin for LCD signals from b2b boards for display	4-lane MIPI DSI, I2C/GPIO, Backlight MIPI Alliance Specification v1.01 MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01	
M.2 (NGFF) PCI Express – Key-E Connector (on bottom)	M.2 PCI Express Key-E connectors for external peripheral connectivity	PCIe1 v2.1 Can support 2230, 2242, 2260 and 2280 M.2 sized cards	For M.2 PCIe add-in cards

Domain	Description	Specification	Usage
CSI Camera connectors	2 x CSI port connector with CLK, GPIOS, CCI	Supports 2 x Camera interfaces via three separate connectors • 2 x MIPI-CSI each 4 lane • External flash driver control • Support for 3D camera configuration • Separate I2C / CCI control MIPI Alliance Specification v1.00 for Camera Serial Interface	For connecting camera accessories.
Power Probe Header	3 pin power probe header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of SOM

The following sections will provide in depth information on each expansion header and connectors on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-X 8M. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

3.8.3 Open-X 8M Power Specification

The Open-X 8M development kit power source is provided by either the 12V DC barrel jack, or the USB Type-C jack. From either the power jack or the USB Type-C jack, the power input branches off into different voltage rails via step down converters on the carrier board and a Power management IC (PMIC) on the SOM. The SOM and carrier board is powered by 3.38V via a Richtek step down converter U400 on the carrier board. The 3.38V is then fed directly to the SOM PMIC. To ensure the SOM is getting powered correctly, a user can monitor the current going into the SOM via the power probe header J600 (see section 3.8.4).

Note that even though the hardware design supports powering the development kit solely from the USB Type-C jack, the software may not support this feature. Please check the release notes for the SW release you are using to confirm whether it is supported. The release notes are available on the product support site.

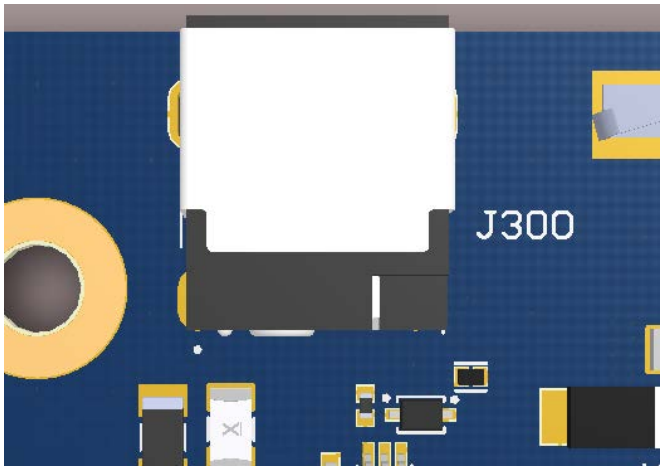

Figure 3-6 12V DC Power Jack J300

Figure 3-7 - USB Type-C J1300

The NXP PF4210 PMIC is used to source various regulated power rails on the SOM.

3.8.4 Power Probe Header J600

Figure 3-8 Power Probe Header J600

The power probe header is used to sense/ monitor the current on the 3.38V power rail going into the SOM. The table below summarizes the pinout of header J600.

Table 3.8.4-1 Power Header Pin-out, J600

Description	Signal	Pin
SOM power positive current sense line	SOM_PWR_SENSE_P	J600[1]
SOM power negative current sense line	SOM_PWR_SENSE_N	J600[2]
GND	GND	J600[3]

To obtain power consumption measurements, the Power Probe Header J600 can be connected to a data acquisition unit (such as a Keithley 2701) and the voltages on the SOM_PWR_SENSE_P/N pins should be captured every few seconds over a test period (typically 30 minutes). The SOM power consumption can then be calculated using the following formula (where Rsense = 5 milliohms):

$$Psom = Vsom_{SOM\_PWR\_SENSE\_N} * \left(\frac{\left(Vsom_{SOM\_PWR\_SENSE\_P} - Vsom_{SOM\_PWR\_SENSE\_N}\right)}{Rsense} \right)$$

3.8.5 Debug Serial UART over USB J800

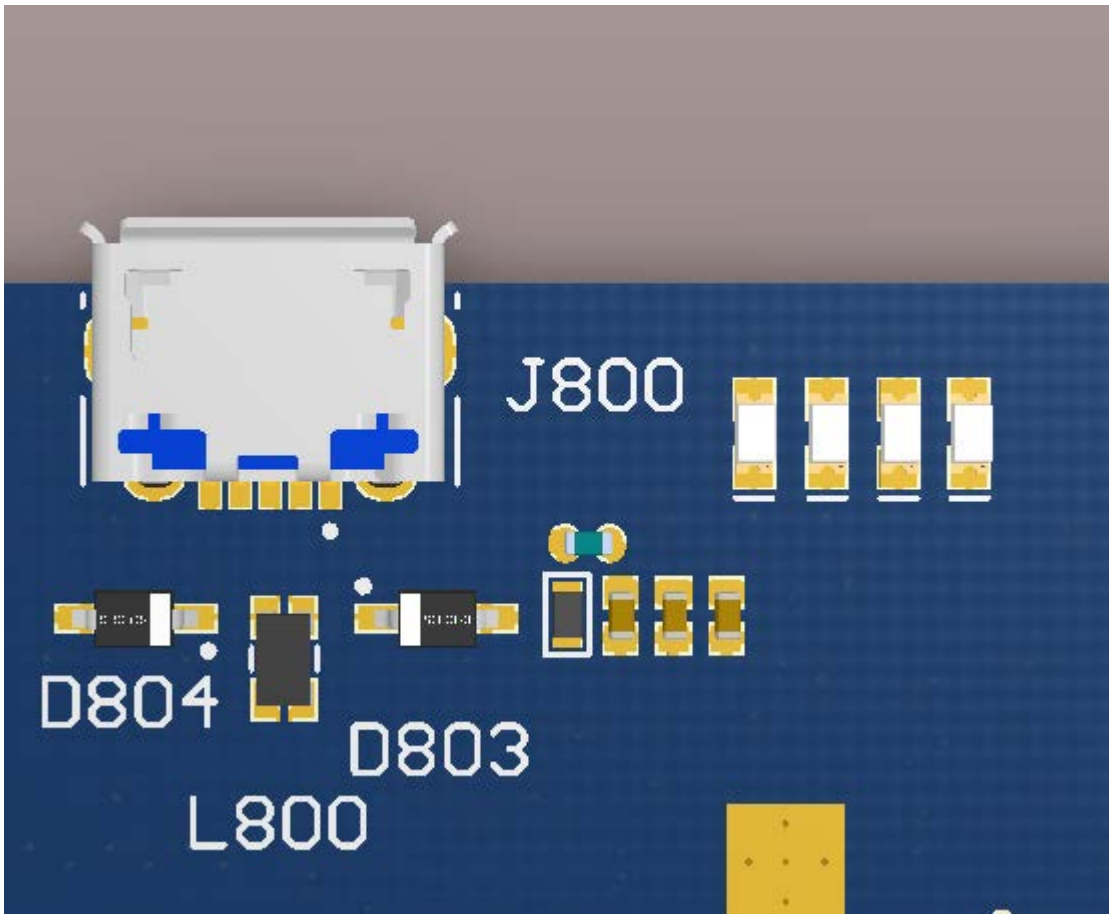

Figure 3-9 Debug UART over USB J800

The UART connection used on the Open-X 8M is a USB micro B connector (J800). The debug UART is available over USB via the SILICON LABS CP2105 chip on the carrier board. UART1_TXD and UART1_RXD are used to output serial debugging information for A53-core. UART2_TXD and UART2_RXD are used to output serial debugging information for M4-core. No RTS or CTS signals are sent from the Processor to the Debug connector as these signals are typically ignored by most applications. To get the serial terminal working with a PC, user needs to ensure that the appropriate SILICON LABS drivers are installed.

The terminal settings are as follows:

Figure 3-10 UART Configuration

Data Rate	115,200 Baud
Bata Bits	8
Parity	None
Stop Bits	1

3.8.6 JTAG Header J801

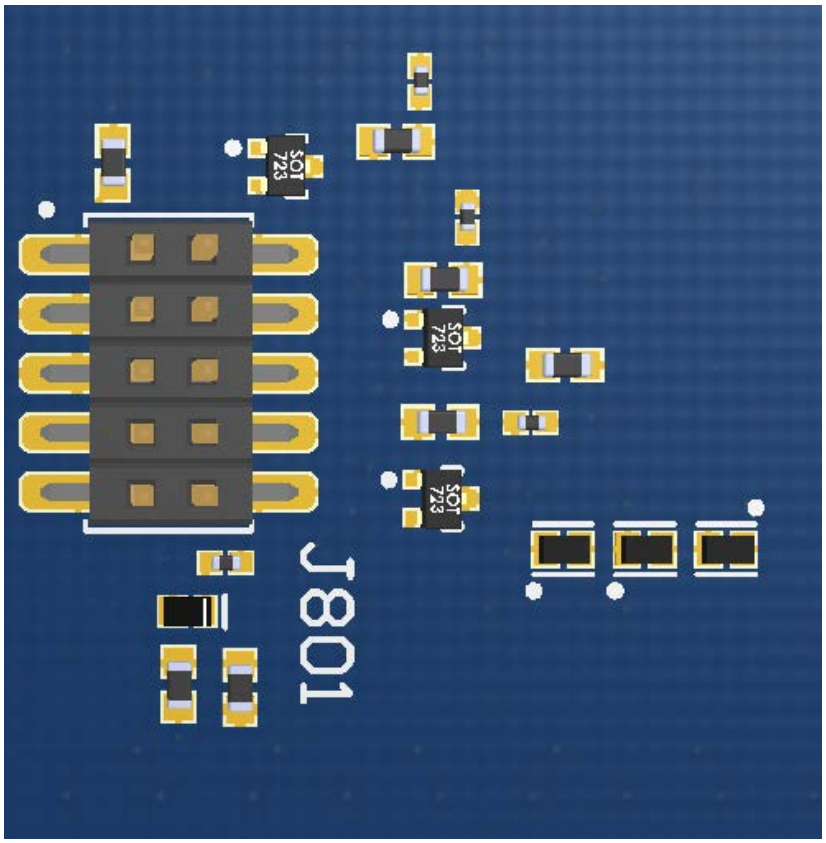

Figure 3-11 JTAG Header J801

This connector provides a JTAG interface to the main processor. The i.MX 8MDQLQ Applications Processor accepts five JATG signals from an attached debugging device on dedicated pins. A sixth pin on the processor accepts a board HW configuration input, specific to the Open-X 8M board.

Note: Intrinsyc does not provide software support for JTAG.

Table 3.8.6-1 JTAG Header Pinout, J801

Description	Signal	Pin NO	Pin NO	Signal	Description
TMS Signal	TMS	J801 [2]	J801 [1]	JTAG_PWR	3V3 JTAG Power detect
TCK Signal	TCK	J801 [4]	J801 [3]	GND	Ground
TDO Signal (Target Data Out)	TDO	J801 [6]	J801 [5]	GND	Ground
TDI Signal (Target Data In)	TDI	J801 [8]	J801 [7]	NC	Not Connected
, not connected	POR_B (NC)	J801 [10]	J801 [9]	TRST_N (NC)	Target RESET_N signal, not connected

3.8.7 MicroSD Card Socket J900

The carrier board has one 4-bit MicroSD card slot on the bottom side which is connected to the SOM via SD2 interface.

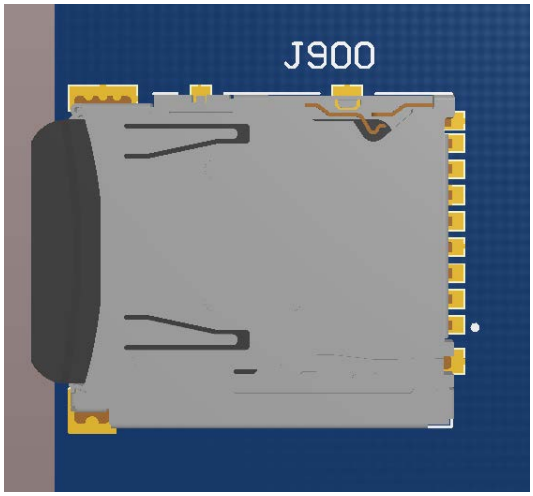

Figure 3-12 SD Card on Carrier Board J900

The SD2 interface is designed to support:

- SD/SDIO standard, up to version 3.0.
- 1.8 V and 3.3 V operation, but do not support 1.2 V operation.
- 4-bit SD and SDIO modes

3.8.8 Buttons and LEDs

There is one user interface, one reset and one power button on the Open-X 8M carrier board.

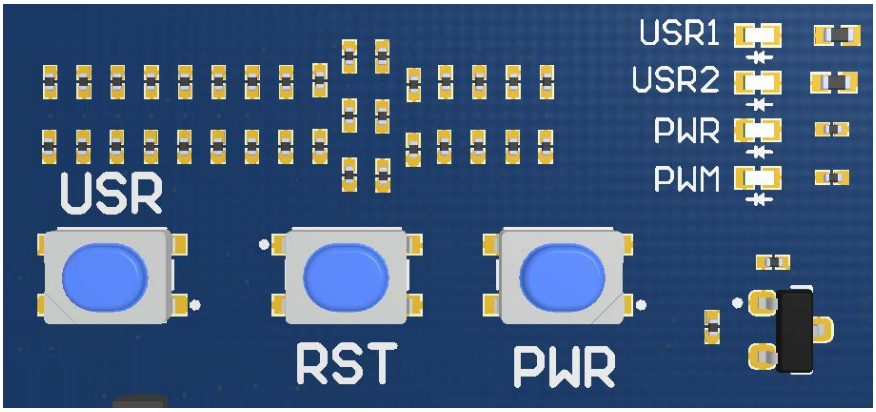

Figure 3-13 Buttons and LEDs

The chip supports the use of a button input signal to request main SoC power state changes (i.e. ON or OFF) from the PMU.

PWR button (S2000) can be configured as debounce, OFF-to-ON time, and max timeout via software. See NXP i.MX8 reference manual (IMX8MDQLQRM).

In the ON state, holding the RST button (S2001) will force all power rails to go low except the VDD_SNVS_3V3 on the Open-X 8M carrier board. The i.MX 8MDQLQ applications processor will be immediately turned off and reinitiate a boot cycle from the OFF state when the RST button is released.

There are two status LEDs and two user LEDs on the carrier board.

The status LEDs have the following functions:

- Green LED ON – The CPU is running in overdrive mode.
- Green LED OFF – The CPU is not in overdrive mode.
- Red LED ON – Power is applied to the 12V DC JACK and power switch (SW400) is ON.
- Red LED OFF – The board has no power applied.

3.8.9 USB Type-C J1300 and Type-A J1301

The i.MX 8MDQLQ Applications Processors contains two USB 2.0/3.0 OTG controllers, with two integrated USB PHYs. On the Open-X 8M development kit, one is used for the USB Type-A host port and the other for the USB Type-C port.

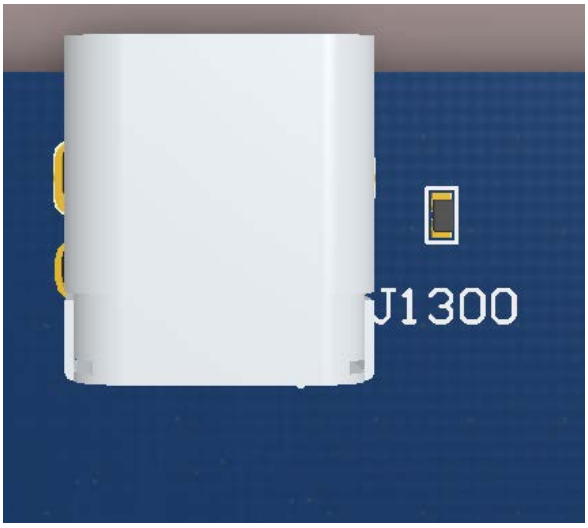

Figure 3-14 - USB Type-C J1300

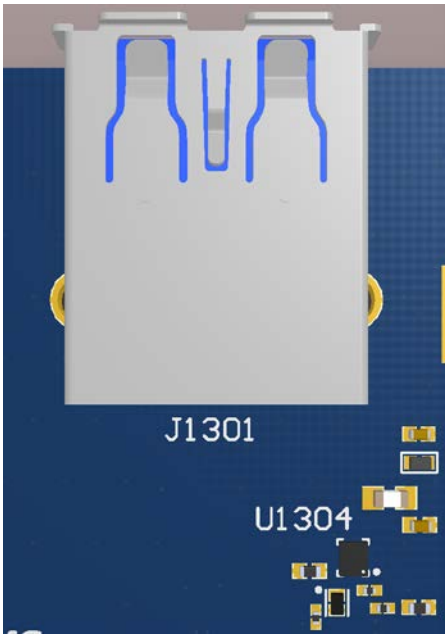

Figure 3-15 - USB Type-A J1301

3.8.10 Audio Stereo Line-out Jack J1200

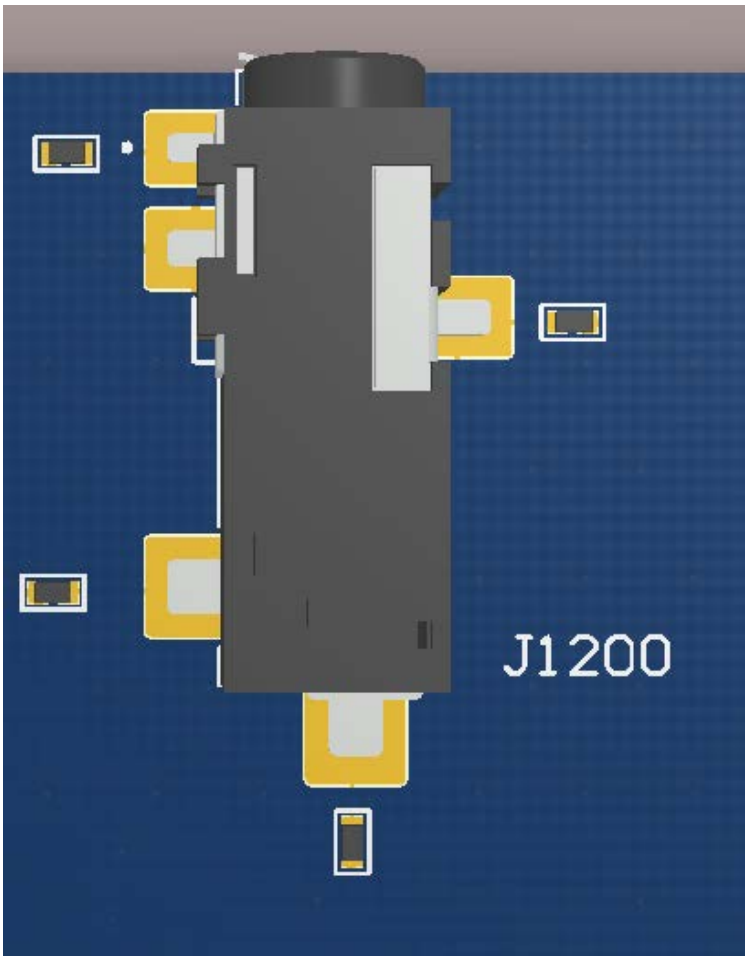

Figure 3-16 3.5mm Audio Line-out Jack J1200

The main Audio DAC used on the Open-X 8M board is the CIRRUS LOGIC Low Power, high quality Stereo DAC, WM8524. The 3.5mm audio jack (J1200) is a 3.5mm CTIA standard pinout TRRS jack.

The 3.5mm jack provides a line level stereo audio output and is not intended drive low impedance speakers or headphones. It is intended to drive amplified devices such as powered PC speakers or sound systems.

3.8.11 Digital Audio Expansion Headers

3.8.11.1 FPC Audio Expansion Connector J1800

Figure 3-17 Audio FPC Header J1800

This header provides the following interfaces:

1. 3 SAI
2. SPDIF
3. I2C
4. NAND

The table below outlines the pinout information of the audio inputs expansion header J1800:

Table 3.8.11-1 Audio Inputs Expansion Header Pinout, J1800

Description	Signal	Pin NO
3V3 or VSYS Voltage	V_AUD	J1800 [1]
3V3 or VSYS Voltage	V_AUD	J1800 [2]
3V3 or VSYS Voltage	V_AUD	J1800 [3]
SAI Master Clock	SAI1_MCLK	J1800 [4]
	GND	J1800 [5]
SAI1 TX Clock	SAI1_TXC	J1800 [6]
	GND	J1800 [7]
SAI1 TX Frame Sync	SAI1_TXFS	J1800 [8]
SAI1 TX Data 0	SAI1_TXD0	J1800 [9]
SAI1 TX Data 1	SAI1_TXD1	J1800 [10]
SAI1 TX Data 2	SAI1_TXD2	J1800 [11]
SAI1 TX Data 3	SAI1_TXD3	J1800 [12]
SAI1 TX Data 4	SAI1_TXD4	J1800 [13]
SAI1 TX Data 5	SAI1_TXD5	J1800 [14]
SAI1 TX Data 6	SAI1_TXD6	J1800 [15]
SAI1 TX Data 7	SAI1_TXD7	J1800 [16]
	GND	J1800 [17]
SAI1 RX Clock	SAI1_RXC	J1800 [18]
SAI1 RX Frame Sync	SAI1_RXFS	J1800 [19]

SAI1 RX Data 0	SAI1_RXD0	J1800	[20]
SAI1 RX Data 1	SAI1_RXD1	J1800	[21]
SAI1 RX Data 2	SAI1_RXD2	J1800	[22]
SAI1 RX Data 3	SAI1_RXD3	J1800	[23]
SAI1 RX Data 4	SAI1_RXD4	J1800	[24]
SAI1 RX Data 5	SAI1_RXD5	J1800	[25]
SAI1 RX Data 6	SAI1_RXD6	J1800	[26]
SAI1 RX Data 7	SAI1_RXD7	J1800	[27]
	GND	J1800	[28]
SAI5 Master Clock	SAI5_MCLK	J1800	[29]
	GND	J1800	[30]
SAI5 RX Clock	SAI5_RXC	J1800	[31]
	GND	J1800	[32]
SAI5 RX Frame Sync	SAI5_RXFS	J1800	[33]
SAI5 RX Data 0	SAI5_RXD0	J1800	[34]
SAI5 RX Data 1	SAI5_RXD1	J1800	[35]
SAI5 RX Data 2	SAI5_RXD2	J1800	[36]
SAI5 RX Data 3	SAI5_RXD3	J1800	[37]
	GND	J1800	[38]
SAI3 Master Clock	SAI3_MCLK	J1800	[39]
	GND	J1800	[40]
SAI3 RX Clock	SAI3_RXC	J1800	[41]
	GND	J1800	[42]
SAI3 RX Frame Sync	SAI3_RXFS	J1800	[43]
SAI3 RX Data 0	SAI3_RXD	J1800	[44]
	GND	J1800	[45]
SPDIF External Lcock or 3V3	SPDIF_EXT_CLK/3V3	J1800	[46]
SPDIF TX	SPDIF_TX	J1800	[47]
SPDIF RX	SPDIF_RX	J1800	[48]
	GND	J1800	[49]
I2C3 Clock	I2C3_SCL	J1800	[50]
I2C3 Data	I2C3_SDA	J1800	[51]
NAND	NAND_nCE3	J1800	[52]
	NAND_nWE	J1800	[53]
	NAND_nWP	J1800	[54]
	NAND_nREADY	J1800	[55]
NAND Data 4	NAND_DATA_4	J1800	[56]
NAND Data 5	NAND_DATA_5	J1800	[57]
NAND Data 6	NAND_DATA_6	J1800	[58]
NAND Data 7	NAND_DATA_7	J1800	[59]
	GND	J1800	[60]

3.8.11.2 Audio Outputs Expansion Headers J1801, J1802, J1803

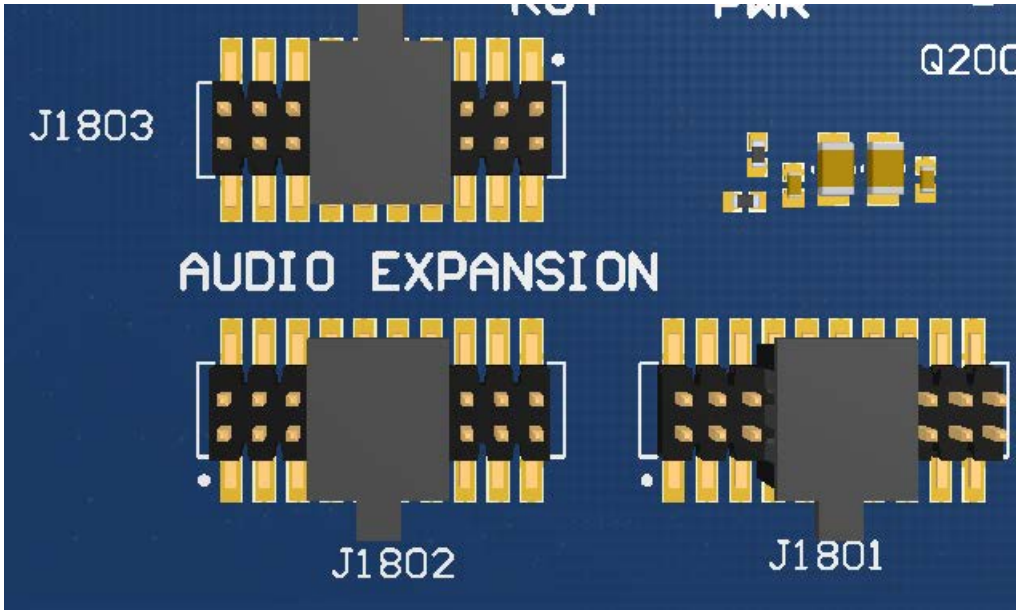

Figure 3-18 Audio Expansion Headers J1801, J1802, J1803

These 0.05mm pitch headers provide all of the same signals that are available on the 60 pin FPC connector and are provided to make it easier for users to connect to individual signals if desired:

1. 3 SAI
2. SPDIF
3. I2C
4. NAND

The table below outlines the pinout information of the audio expansion headers:

Table 3.8.11-2 Audio Outputs Expansion Headers Pinout, J1801, J1802, J1803

J1801

Signal	Pin NO	Pin NO	Signal
V_AUD	J1801 [1]	J1801 [2]	GND
SAI1_RXFS	J1801 [3]	J1801 [4]	SAI1_RXD5
SAI1_RXC	J1801 [5]	J1801 [6]	SAI1_RXD4
SAI1_TXFS	J1801 [7]	J1801 [8]	SAI1_RXD3
SAI1_TXD0	J1801 [9]	J1801 [10]	GND
SAI1_TXD1	J1801 [11]	J1801 [12]	SAI1_RXD2
SAI1_TXD2	J1801 [13]	J1801 [14]	SAI1_RXD1
SAI1_TXD3	J1801 [15]	J1801 [16]	SAI1_RXD0
SAI1_TDC	J1801 [17]	J1801 [18]	SAI1_TXD5
GND	J1801 [19]	J1801 [20]	GND

J1802

Signal	Pin NO	Pin NO	Signal
V_AUD	J1802 [1]	J1802 [2]	GND
SAI1_MCLK	J1802 [3]	J1802 [4]	SPDIF_EXT_CLK
SAI1_RXD6	J1802 [5]	J1802 [6]	SAI5_RXC
SAI1_RXD7	J1802 [7]	J1802 [8]	SAI5_RXFS
SPDIF_TX	J1802 [9]	J1802 [10]	GND
SPDIF_TX	J1802 [11]	J1802 [12]	SAI1_RXD3
SAI1_TXD7	J1802 [13]	J1802 [14]	SAI1_RXD2
SAI1_TXD6	J1802 [15]	J1802 [16]	SAI1_RXD1
SAI1_TXD4	J1802 [17]	J1802 [18]	SAI1_RXD0
GND	J1802 [19]	J1802 [20]	GND

J1803

Signal	Pin NO	Pin NO	Signal
V_AUD	J1803 [1]	J1803 [2]	GND
SAI3_MCLK	J1803 [3]	J1803 [4]	SAI5_MCLK
SAI3_RXC	J1803 [5]	J1803 [6]	NAND_nCE3
SAI3_RXD	J1803 [7]	J1803 [8]	NAND_nREADY
SAI3_RXFS	J1803 [9]	J1803 [10]	GND
NAND_nWE	J1803 [11]	J1803 [12]	NAND_DATA_7
NAND_nWP	J1803 [13]	J1803 [14]	NAND_DATA_6
I2C3_SCL	J1803 [15]	J1803 [16]	NAND_DATA_5
I2C3_SDA	J1803 [17]	J1803 [18]	NAND_DATA_4
GND	J1801 [19]	J1801 [20]	GND

3.8.12 On Board PCB WLAN Antenna

The Open-X 8M carrier board has two dual-band (2.4GHz & 5GHz) WLAN/Bluetooth PCB trace antennas. These antennas connect to the QCA6174A WiFi module on the SOM via coaxial cables that attach to MH4L receptacles. The Open-X 8M Development Kit comes complete with the two coaxial cables installed.

The antennas connect to the SOM in the following configuration:

- WLAN/BT ANT 1 on the carrier board connects to ANT1 on the WiFi module
- WLAN/BT ANT 2 on the carrier board connects to ANT2 on the WiFi module

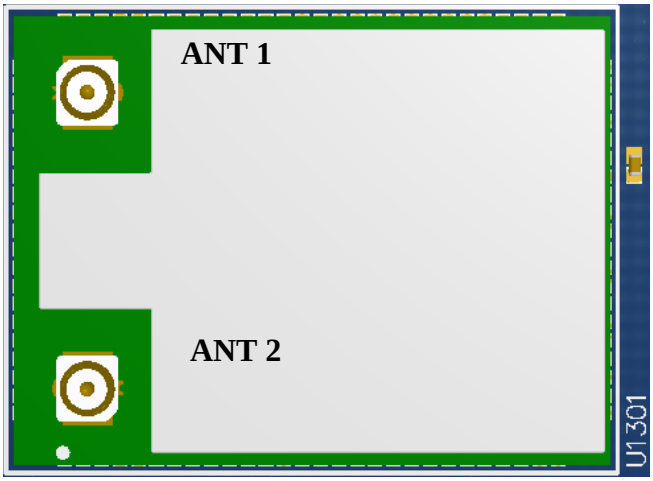

Figure 3-19 QCA6174A Module on SOM

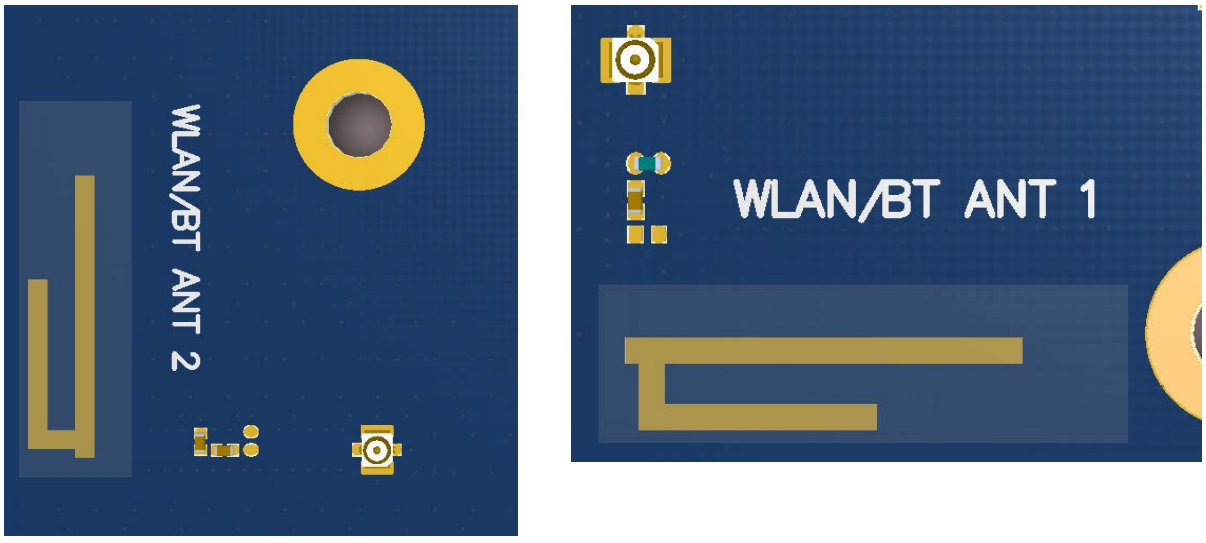

Figure 3-20 On Board PCB Antennas

3.8.13 Open-X Display Interfaces

The display output options for the Open-X 8M Development Kit consists of:

- An HDMI Type-A connector
  - HDMI 2.0a (4K 60Hz)
- A 100-pin display connector that supports:
  - MIPI DSI (up to 1080 x 1024 at 60Hz)
  - Touch screen capacitive panels via I2C, SPI, and interrupts (up to two devices)

The Open-X development platform can support the following display combinations:

MIPI DSI	1 x 4lane DSI Display 1080 x 1024 at 60Hz
HDMI	• HDMI 2.0a supporting one display: resolution up to 4096 x 2160 at 60 Hz • 20+ Audio interfaces 32-bit @ 384 kHz fs, with Time Division Multiplexing (TDM)

3.8.13.1 HDMI Connector J1000

The on-board HDMI Type-A connector enables the Open-X development platform to connect to an external HDMI monitor or television via a standard HDMI cable. The Open-X 8M can support up to 4K UHD (4096 x 2160 at 60 Hz) and HDMI 2.0 a.

Please note that the Open-X 8M Development kit is for evaluation purposes only and may not be HDMI standard compliant.

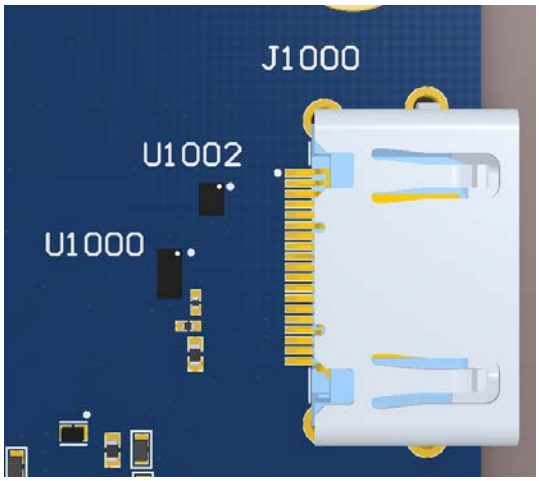

Figure 3-21 HDMI connector on Carrier Board J1000

3.8.13.2 Display Connector J1700

The 100-pin display connector provides the following features and pin-outs that enables the development kit to connect to a MIPI DSI display panel or other device:

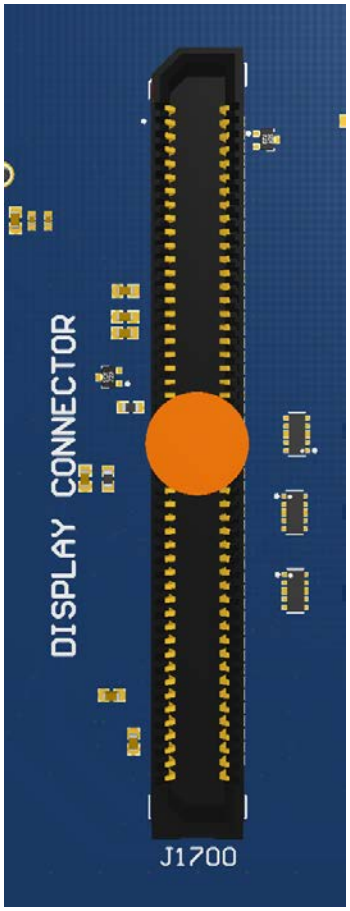

Figure 3-22 MIPI Display Connector on Carrier Board J1700

The display connector provides the following interfaces:

- DSI – 1 x 4-lane MIPI DSI interface
- 5V, 12V, 1.8V and 3.0V voltage rails
- Touch Panel Support – supports I2C touch controllers
- Additional GPIOs for general purposes available.

Note: Please refer to the carrier board schematic and Display Board Design Guide document when designing a custom display interface board.

3.8.13.3 J1700 Pinout

The below table shows the pinout for J1700 connector:

Pin	Signal	Description
1,3,5,10,11,12,13,16,17, 18,19,21,22,23,24,25,28, 30,33,34,35,36,37,40,41, 42,43,47,51,53,59,63,67, 69,71,73,75,76,77,78,79, 81,82,83,84,88,90,92,94, 96,98,100	NU	Not Connected
4	DSI_EN	Enable GPIO for DSI display
6	DSI_BL_PWM	Backlight PWM
7	DSI_TS_SDA	Touch Screen I2C Data
9	DSI_TS_SCL	Touch Screen I2C Clock
15	TS0_RESETn	Touch Screen Reset Output
27,31,57	NVCC_1V8	
39	DSI_TS_nINT	Touch Screen Sample Interrupt
45	DSI_LCD_TE	CMOS TE Trigger
46	MIPI_DSI_LANE0_N	DSI Data Lane 0
48	MIPI_DSI_LANE0_P	DSI Data Lane 0
49	MIPI_DSI_RESETn	
52	MIPI_DSI_LANE1_N	DSI Data Lane 1
54	MIPI_DSI_LANE1_P	DSI Data Lane 1
55	VDDIO_TP_1V8	
58	MIPI_DSI_CLK_N	DSI Clock Lane
60	MIPI_DSI_CLK_P	DSI Clock Lane
61	DISP_3V0	
64	MIPI_DSI_LANE2_N	DSI Data Lane 2
66	MIPI_DSI_LANE2_P	DSI Data Lane 2
70	MIPI_DSI_LANE3_N	DSI Data Lane 3
72	MIPI_DSI_LANE3_P	DSI Data Lane 3
89	DC_IN_12V	
91,93,95	DCDC_5V	
2,8,14,20,26,29,32,38,44, 50,56,62,65,68,74,80,85, 86,87,97,99	GND	

The optional Open-X display board accessory (part number: QC-DB-G00005) is an additional PCB that mates with the display connector J1700 on the carrier board. This board allows users to interface with the development kit via the LCD display panel and touchscreen.

Note: The display board comes as an optional add-on to the Open-X 8M development kit. To purchase this, please visit http://shop.intrinsyc.com or contact Intrinsyc at sales@intrinsyc.com for details.

3.8.14 Ethernet Connector J1400

There is one Gigabit Ethernet port on the i.MX 8MDQLQ processor. The developer can use the Ethernet connector to send/receive the ENET signals. The Ethernet PHY of the Open-X 8M carrier board is provided by the Qualcomm AR8031 Ethernet transceiver chip (U1400) which interfaces to the i.MX 8M processor via standard RGMII Ethernet signals.

The processor takes care of all Ethernet protocols at the MAC layer and above. The PHY is only responsible for the Link Layer formatting. The PHY receives the clock signal from the ENET_TXC pin of i.MX 8MDQLQ processor.

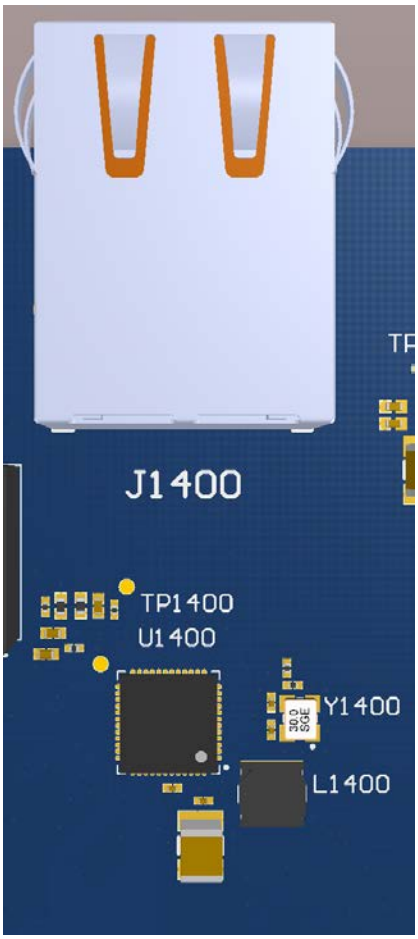

Figure 3-23 Gigabit Ethernet RJ45 Jack J1400

3.8.15 M.2 Key E PCI Express Slot J1100

The M.2 Key E PCI Express slot (J1100) used on the Open-X 8M development kit is a standard PC style half-height card slot. It allows for external peripheral connectivity such as Wi-Fi / Bluetooth, or PCIe based audio / video processors. Supported Card sizes are: 2230, 2245, 2260 and 2280. Mounting holes are labelled on the top side of the PCB. In addition to being able to establish external connectivity, the connector provides access to the PCIE2 interface, which is routed from the SOM.

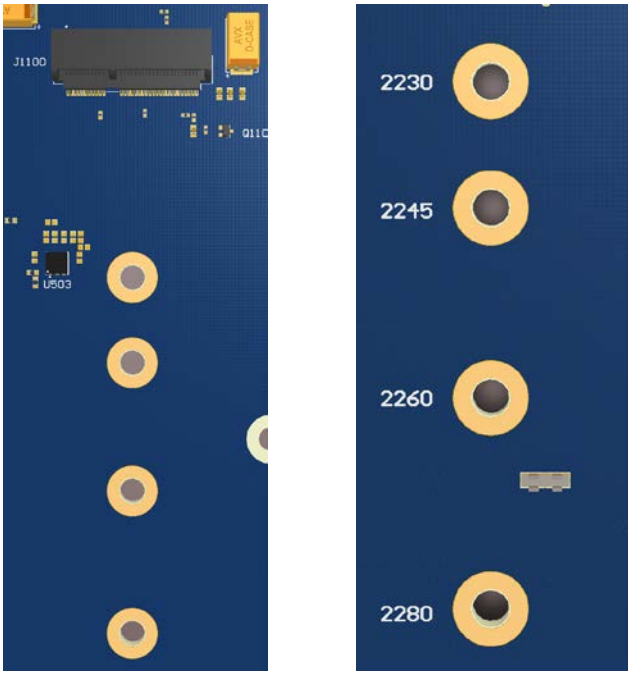

Figure 3-24 PCIe Connector and Mounting Holes J1100

The connector makes the following interfaces available: SD2, I2C, PCM, UART PCIE2 and USB2. The USB2 connection is routed to the USB Type-A connector by default but can be made available to the PCIe socket by switching the USB select switch (SW2000) as shown below:

Figure 3-25 USB Select Switch for PCIE

3.8.16 Camera connectors

The Open-X 8M development kit supports two 4-lane MIPI camera interfaces via two separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 2 x 4 lane MIPI CSI signals
- Supports all CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.

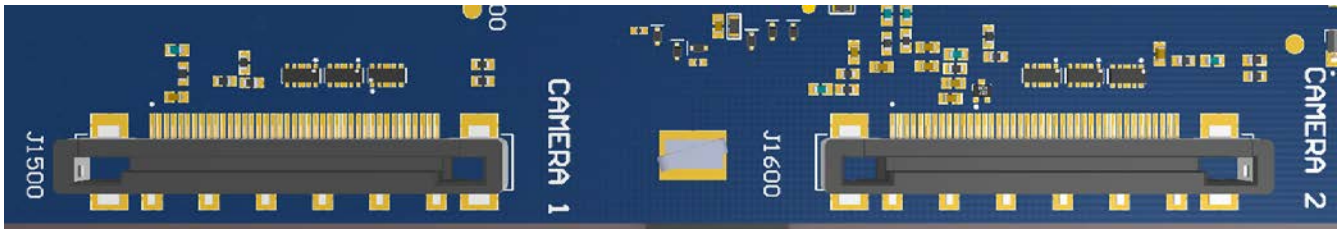

Figure 3-26 Camera Connectors J600, J1500

Table 3.8.16-1 below outlines the pinouts of these connectors

Table 3.8.16-1. MIPI CSI Camera Connector Pinouts (J1500, J1600)

Pin#	CAM1 (J1500)	CAM2 (J1600)	Description
1	NVCC_3V3	NVCC_3V3	Power output. Connected to main +3.3V
2	NVCC_3V3	NVCC_3V3	Power output. Connected to main +3.3V
3	NVCC_3V3	NVCC_3V3	Power output. Connected to main +3.3V
4,11, 19,22, 25,28 31,34,	GND	GND	Ground
5	CAM_2V85	CAM_2V85	Power output. Connected to CAM LDO U502 regulators. Default is +2.85V. Maximum current 1A
6	CAM1_DVDD	CAM2_DVDD	Power output. Connected to U500, U501 LDO regulators. Default is +1.12V. VCAM_1V5 can be used instead.
7	VCAM_2V8	VCAM_2V8	Power output. Connected to SOM PMIC VGEN6. Default is +2.8V. Maximum current 200mA
8	VCAM_2V8	VCAM_2V8	Power output. Connected to SOM PMIC VGEN6. Default is +2.8V. Maximum current 200mA

Pin#	CAM1 (J1500)	CAM2 (J1600)	Description
9	NVCC_1V8	NVCC_1V8	Power output. Connected to PMIC SW4 switch output. Default is +1.8V. Maximum current 300mA
10	NVCC_1V8	NVCC_1V8	Power output. Connected to PMIC SW4 switch output. Default is +1.8V. Maximum current 300mA
13	CSI_nRST_1V8	CSI_nRST_1V8	Output. Connected to i.MX 8M8 gpio1.IO[6]. Default use is for camera reset.
14	CAM1_nPWDN_1V8	CAM1_nPWDN_1V8	Output. Connected to i.MX 8M8 gpio1.IO[3]. Default use is for camera standby.
15	CSI_I2C_SCL	CSI_I2C_SCL	Output. Connected to i.MX 8M8 I2C3 bus. Default use is for camera CSI I2C clock interface.
16	CSI_I2C_SDA	CSI_I2C_SDA	Input / output. Connected to i.MX 8M8 I2C3 bus. Default use is for camera CSI I2C data interface.
17	CAM1_MCLK0	CAM2_MCLK0	Output. Connected to i.MX 8M8 gpio1.IO[15]. Default use is for camera master clock. Maximum 24MHz.
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
12,18,35,36,37,38,39,40,41	NU	NU	Not Used

Note: A connection from the camera connectors on the carrier board to the camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

The table below shows the combinations of camera usage for different use cases

Table 3.8.16-2. MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane

3.8.17 3-Pin 5V DC Fan Connector

The carrier board has one 5V DC fan interface. J700 is a standard TX3 style connector (part number Molex 0022232031) which gives greater flexibility for fan selection. SW700 can be used to shut off the fan when it is not in use. The tachometer is not routed back to the SOM and the fan uses a constant 5V DC so speed control is not an option. If these features are required, contact Intrinsyc for customization.

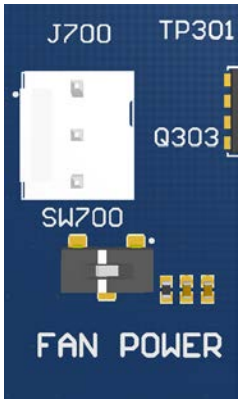

Figure 3-27 3-Pin 5V DC Fan Connector J700

The table below shows the pinout of the fan connector:

Table 3.8.17-1 3 Pin 5V DC Fan Header Pin-out J700

Pin	Connection
1	GND
2	5V DC
3	GND