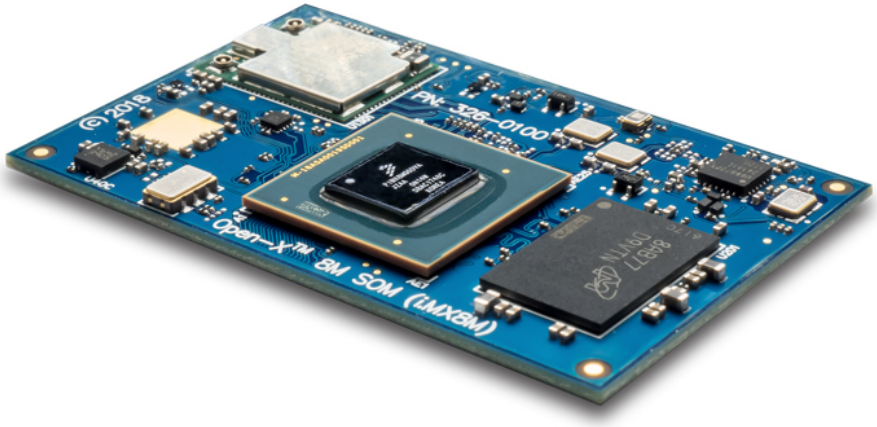

Intrinsyc Open-X™ 8M SOM
HW Device Specification

[Document: ITC-01RND1319-SOM-DS Version: 1.0]

IDENTIFICATION

Document Title	Intrinsyc Open-X™ 8M SOM HW Device Specification
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History

REVISION	DATE	DESCRIPTION	PAGES
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Table of Contents

1. INTRODUCTION

This document applies to the Open-X 8M SOM.

1.1 Purpose

The purpose of this document is to provide specifications and technical information for the Intrinsyc Open-X 8M System-On-Module (SOM).

For background information on the SOM and associated development kit, please refer to:

https://www.intrinsyc.com/computing-platforms/open-x-8m-system-on-module-som/
https://www.intrinsyc.com/imx-embedded-development-kits/open-x-8m-development-kit/

1.2 Scope

This document presents specifications and technical information for the Intrinsyc Open-X 8M SOM.

1.3 Intended Audience

This document is intended for OEMs interested in designing a product based on the Open-X 8M SOM.

1.4 Acronyms and Abbreviations

Acronym / Abbreviation	Definition
ANT	ANTenna
BOM	Bill Of Materials
BT	BlueTooth
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMI	Electro-Magnetic Interference
EN	ENable
ERM	Eccentric Rotating Mass
ESD	Electro-Static Discharge
GND	GrouND
GPIO	General Purpose I/O
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	INTerrupt
JTAG	Joint Test Action Group
LDO	Low Drop-Out
LNA	Low Noise Amplifier
LRM	Linear Resonant Actuator
LTE	Long-Term Evolution
MDP	Mobile Display Port
MI2S	Mobile Inter-IC Sound
MIC	MICrophone
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PWM	Pulse-Width Modulation
RF	Radio Frequency
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SDC	Secure Digital Interface
SOM	System On Module
SPI	Serial Peripheral Interface
SSC	Snapdragon Sensor Core
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UIM	User Interface Module
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

1.5 Signal Name Suffix

Suffix	Definition
_N	Indicates that the signal is ACTIVE LOW
_P/N	Identifies the two signals comprising a differential pair

2. REFERENCE DOCUMENTS

This section lists any parent and supplementary documents for the Open-X 8M SOM Technical Note. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-X 8M SOM

2.2 Reference Documents

These documents are available on the Open-X 8M Technical Portal at:

http://tech.intrinsyc.com (product registration required)

REFERENCE	TITLE
R-1	Open-X 8M Development Kit Schematics (SOM, Carrier)
R-2	Open-X 8M Development Kit Bill of Materials
R-3	Open-X 8M Development Kit User Guide
R-4	ITCNFA324 Module Certification OEM Integrator Instructions

3. SUMMARY OF FEATURES

The Open-X 8M SOM is an compact (55mmx35mm) production-ready SOM ideal for powering anything from consumer home video/audio to industrial building automation products. The feature-rich SOM, with industry-leading video/audio features and high speed Wi-Fi, is ideal for streaming devices, voice control applications, and human-machine interface solutions.

The Open-X 8M SOM offers high quality video playback with full 4K UHD and HDR along with the highest level of pro-audio fidelity. The wide range of interfaces, including HDMI 2.0a, two USB 3.0, one PCIe, Gigabit Ethernet, and pre-certified dual-band 2x2 MU-MIMO WLAN make the SOM suitable for a wide range of embedded and IoT products.

3.1 SOM Block Diagram

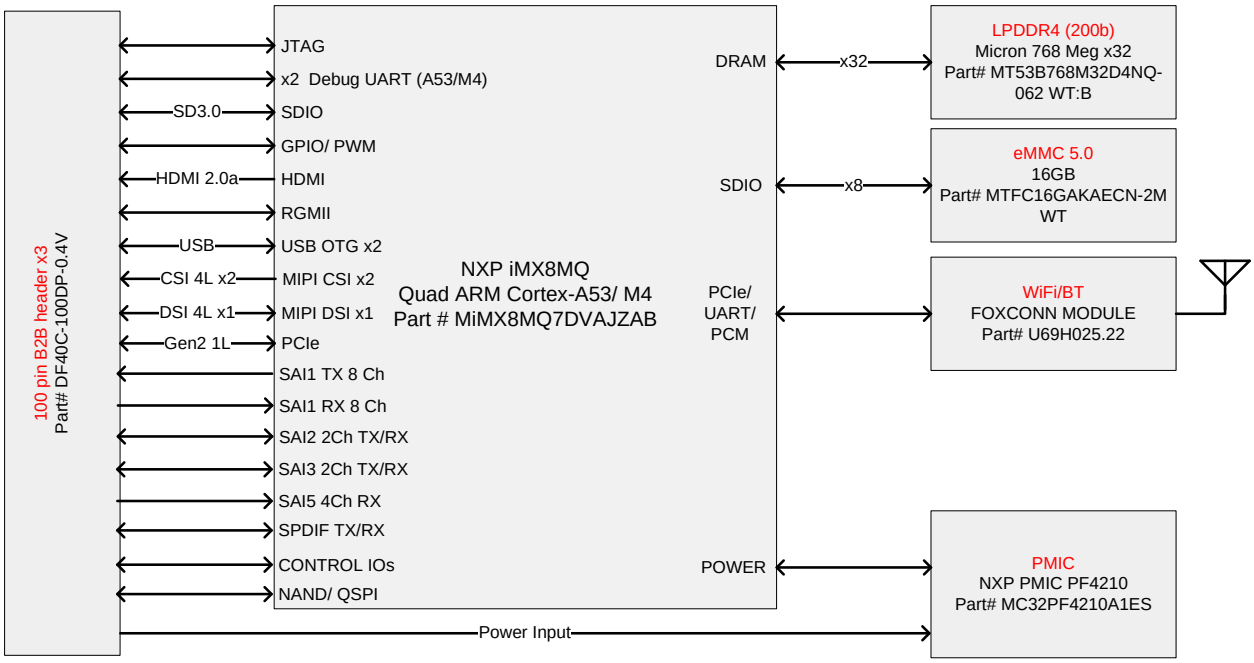

Figure 1 - Open-X 8M SOM Block Diagram

3.2 SOM Technical Specifications

Table 1 - Open-X 8M SOM Functional Specifications

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	MiMX8MQ6DVAJZAB	NXP's i.MX 8M family processor.	Quad ARM Cortex®-A53 and ARM Cortex®-M4 cores, 1.5GHz

Subsystem / Connectors	Feature Set	Description	Specification
	PMIC (PF4210)	NXP PMIC designed for i.MX 8M Processors	NA
Memory	3GB LPDDR4	Memory	Up to 1600MHz LPDDR4 Supported via 1x32bit DRAM channel
	16 GB eMMC	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	Micron eMMC.
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via QCA6174A-1 – PCIe	QCA6174A-1 Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac – 20/40 MHz at 2.4 GHz, 20/40/80 MHz at 5.0 GHz via QCA6174A-1 over PCIe1. Full 2x2 antenna configuration.
	BT V4.1 - 2.4 GHz via QCA6174A-1 – UART / PCM	QCA6174A-1 Wi-Fi + BT Combo Chip	Support BT 4.1 + HS, BLE and backward compatible with BT 1.x, 2.x + EDR
RF Interfaces	2xWLAN / BT MH4	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
Audio Interfaces	4 x SAI	Synchronous Audio Interfaces	SAI1 8ch TX/RX SAI2 2ch TX/RX SAI3 2ch TX/RX SAI5 4ch RX
	1 x SPDIF	Digital Audio Interface	SPDIF TX/RX

Interfaces	2 x MIPI CSI	Camera Connectors CSI1, CSI2	MIPI Alliance Specification v1.0
	2 x USB 2.0/ 3.0 OTG		USB3.0 Standard
	1 x MIPI DSI		MIPI Alliance Specification v1.01. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01
	2 x PCIe 1Lane Gen2		PCI Express Specification, Rev 2.1
	1 x Gigabit Ethernet	RGMII interface	
	1 x HDMI 2.0a	HDMI capable of 4K 60Hz content	HDMI 2.0a
	3 x Memory / Storage	1 x 8 bit NAND 1 x 4 bit QSPI 1 x 4 bit SDIO	JEDEC/MMC standard version 5.0, SD 3.0
	2 x I2C	I2C1, I2C3	
	2 x Debug UART	1x Enhanced UART for A53 1x Standard UART for M4	Enhanced and Standard UART
	1 x JTAG		

4. I/O DEFINITIONS

4.1 Location of Major Components

RF antenna connectors for the SOM are located on the top side of the module.

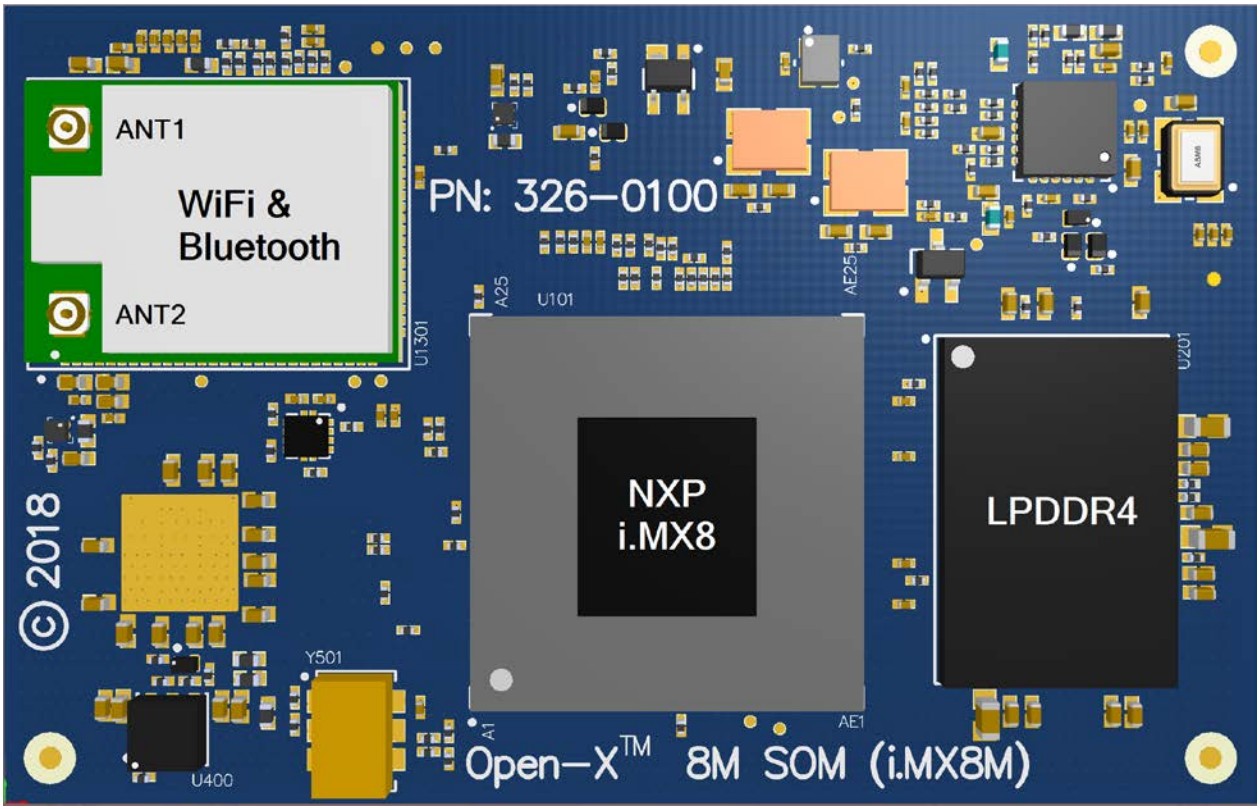

Figure 2- Open-X 8M SOM (Top View)

The SOM mates to the carrier board via connectors JT1200, JT1202, and JT1203; all located on the bottom side of the SOM. The relative location of these connectors is shown in the picture below. Key dimensions are provided in later sections of this document.

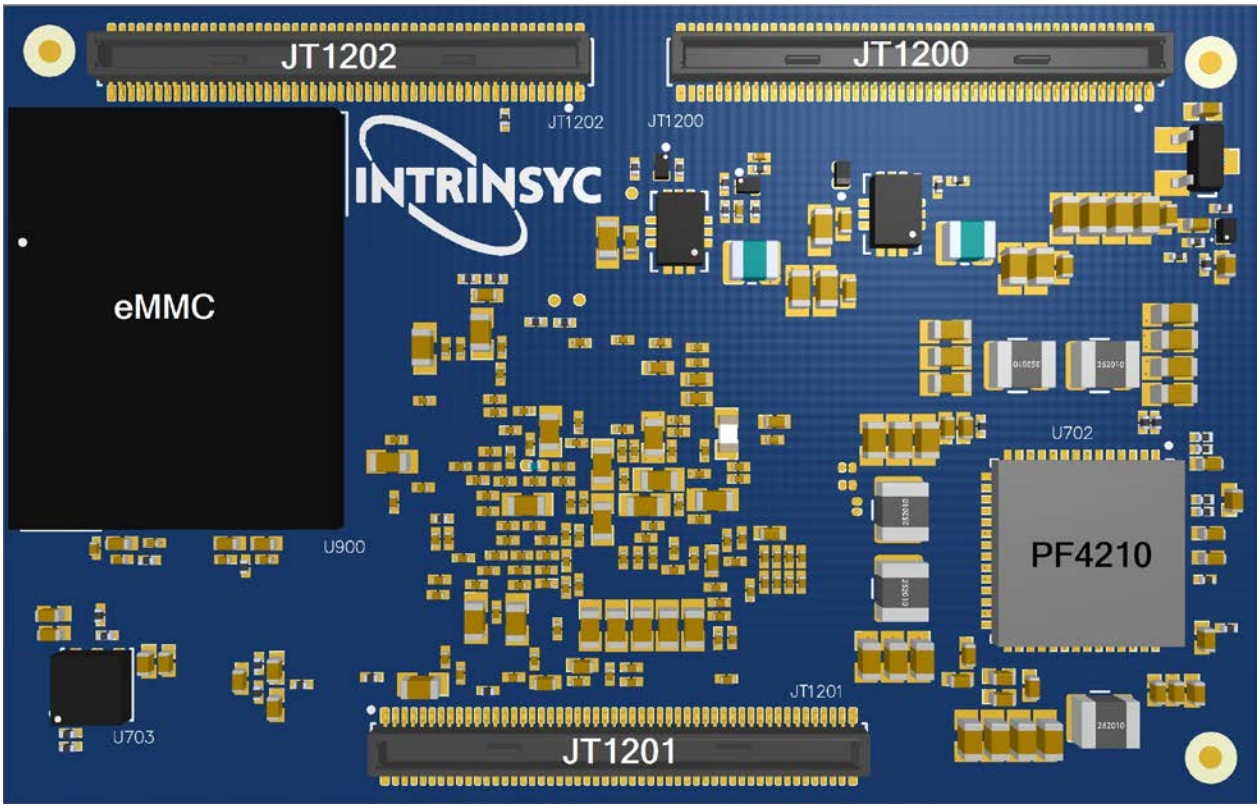

Figure 3 - Open-X 8M SOM (Bottom View) with Pin 1 Locations

4.2 Board-to-Board Connections

This section describes the signals available on the SOM 300 board-to-board connections. Pin-out information is provided here for reference. Note that the SOM schematic is the controlling document. In the event of pin-out difference(s) between this document and the SOM schematic, the SOM schematic shall take precedence.

Table 2 - SOM Pinout

Connector (Pin #)	Pin Name	Description
JT1200 (1)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (2)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (3)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (4)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (5)	SOM_SYS_PWR	Main input power rail for the SOM.
JT1200 (6)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (7)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (8)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (9)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (10)	SOM_SYS_PWR	Main input power rail for the SOM

JT1200 (11)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (12)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (13)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (14)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (15)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (16)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (17)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (18)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (19)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (20)	SPDIF_EXT_CLK	SPDIF External Clock Input
JT1200 (21)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (22)	SPDIF_TX	SPDIF TX line
JT1200 (23)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (24)	SPDIF_RX	SPDIF RX line
JT1200 (25)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (26)	REF_CLK_32K	Auxiliary Reference clock at 32kHz
JT1200 (27)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (28)	GND	Ground
JT1200 (29)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (30)	CLKO_25MHz	Auxiliary Clock at 25MHz
JT1200 (31)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (32)	GND	Ground
JT1200 (33)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (34)	MIPI_CSI2_CLK_P	MIPI CSI 2 clock positive
JT1200 (35)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (36)	MIPI_CSI2_CLK_N	MIPI CSI 2 clock negative
JT1200 (37)	SOM_SYS_PWR	Main input power rail for the SOM
JT1200 (38)	GND	Ground
JT1200 (39)	GND	Ground
JT1200 (40)	MIPI_CSI2_LANE1_P	MIPI CSI 2 data lane 1 positive
JT1200 (41)	USB2_SS_RX_N	USB port 2 super-speed RX negative
JT1200 (42)	MIPI_CSI2_LANE1_N	MIPI CSI 2 data lane 1 negative
JT1200 (43)	USB2_SS_RX_P	USB port 2 super-speed RX positive
JT1200 (44)	GND	Ground
JT1200 (45)	USB2_SS_TX_N	USB port 2 super-speed TX negative
JT1200 (46)	MIPI_CSI2_LANE2_P	MIPI CSI 2 data lane 2 positive
JT1200 (47)	USB2_SS_TX_P	USB port 2 super-speed TX positive
JT1200 (48)	MIPI_CSI2_LANE2_N	MIPI CSI 2 data lane 2 negative
JT1200 (49)	USB2_HS_D_N	USB port 2 high-speed negative
JT1200 (50)	GND	Ground
JT1200 (51)	USB2_HS_D_P	USB port 2 high-speed positive

JT1200 (52)	MIPI_CSI1_CLK_N	MIPI CSI 1 clock negative
JT1200 (53)	USB2_ID	USB2 OTG ID line
JT1200 (54)	MIPI_CSI1_CLK_P	MIPI CSI 1 clock positive
JT1200 (55)	USB1_ID	USB1 OTG ID line
JT1200 (56)	GND	Ground
JT1200 (57)	USB1_SS_RX_N	USB port 1 super-speed RX negative
JT1200 (58)	MIPI_CSI1_LANE0_N	MIPI CSI 1 data lane 0 negative
JT1200 (59)	USB1_SS_RX_P	USB port 1 super-speed RX positive
JT1200 (60)	MIPI_CSI1_LANE0_P	MIPI CSI 1 data lane 0 positive
JT1200 (61)	USB1_SS_TX_N	USB port 1 super-speed TX negative
JT1200 (62)	GND	Ground
JT1200 (63)	USB1_SS_TX_P	USB port 1 super-speed TX positive
JT1200 (64)	MIPI_CSI1_LANE2_P	MIPI CSI 1 data lane 2 positive
JT1200 (65)	USB1_HS_D_P	USB port 1 high-speed positive
JT1200 (66)	MIPI_CSI1_LANE2_N	MIPI CSI 1 data lane 2 negative
JT1200 (67)	USB1_HS_D_N	USB port 1 high-speed negative
JT1200 (68)	GND	Ground
JT1200 (69)	USB1_VBUS	USB1 VBUS sense line
JT1200 (70)	PWM_LED	Tied to VDD_ARM_0V9 to show the state of DVFS.
JT1200 (71)	USB1_VBUS	USB1 VBUS sense line
JT1200 (72)	PCIe_nDIS	Power control for PCIe voltage rail.
JT1200 (73)	GND	Ground
JT1200 (74)	GND	Ground
JT1200 (75)	MIPI_CSI2_LANE3_N	MIPI CSI 2 data lane 3 negative
JT1200 (76)	CLKO2	
JT1200 (77)	MIPI_CSI2_LANE3_P	MIPI CSI 2 data lane 3 positive
JT1200 (78)	GND	Ground
JT1200 (79)	GND	Ground
JT1200 (80)	I2C1_SCL	I2C 1 Clock
JT1200 (81)	MIPI_CSI2_LANE0_N	MIPI CSI 2 data lane 0 negative
JT1200 (82)	I2C1_SDA	I2C 1 Data
JT1200 (83)	MIPI_CSI2_LANE0_P	MIPI CSI 2 data lane 0 positive
JT1200 (84)	GND	Ground
JT1200 (85)	GND	Ground
JT1200 (86)	UART3_CTS	UART 3 CTS
JT1200 (87)	MIPI_CSI1_LANE3_N	MIPI CSI 1 data lane 3 negative
JT1200 (88)	UART3_RXD	UART 3 RX
JT1200 (89)	MIPI_CSI1_LANE3_P	MIPI CSI 1 data lane 3 positive
JT1200 (90)	GND	Ground
JT1200 (91)	GND	Ground
JT1200 (92)	GND	Ground

JT1200 (93)	MIPI_CSI1_LANE1_N	MIPI CSI 1 data lane 1 negative
JT1200 (94)	UART3_TXD	UART 3 TX
JT1200 (95)	MIPI_CSI1_LANE1_P	MIPI CSI 1 data lane 1 positive
JT1200 (96)	UART3_RTS	UART 3 RTS
JT1200 (97)	GND	Ground
JT1200 (98)	GND	Ground
JT1200 (99)	VCAM_1V5	1.5V Voltage rail for CSI Camera
JT1200 (100)	CSI_P2_PWDN	MIPI CSI Power Control for CSI2.
JT1201 (1)	JTAG_nTRST	JTAG_nTRST input
JT1201 (2)	GND	Ground
JT1201 (3)	JTAG_MOD	JTAG MOD input to i.MX8 processor
JT1201 (4)	DSI_TS_nINT	DSI Touch Screen Interrupt
JT1201 (5)	BOOT_MODE0	Boot mode 0 pin for boot configuration
JT1201 (6)	HDMI_DDC_SCL	HDMI DDC Clock
JT1201 (7)	BOOT_MODE1	Boot mode 1 pin for boot configuration
JT1201 (8)	HDMI_DDC_SDA	HDMI DDC Data
JT1201 (9)	JTAG_TMS	JTAG TMS input to i.MX8 processor
JT1201 (10)	GND	Ground
JT1201 (11)	JTAG_TDI	JTAG TDI output from i.MX8 processor
JT1201 (12)	DSI_BL_PWM	DSI Display Back Light PWM control
JT1201 (13)	JTAG_TCK	JTAG TCK input to i.MX8 processor
JT1201 (14)	VCAM_2V8	2.8V Voltage rail for Camera interface
JT1201 (15)	JTAG_TDO	JTAG TDO input to i.MX8 processor
JT1201 (16)	PCIe_nWAKE	Wake signal for PCIe Expansion Card
JT1201 (17)	HDMI_CEC	HDMI Consumer Electronic Control
JT1201 (18)	DSI_EN	DSI Display Enable
JT1201 (19)	HDMI_HPD	HDMI Hot Plug Detect
JT1201 (20)	CSI_P1_PWDN	CSI 1 Power Down
JT1201 (21)	GND	Ground
JT1201 (22)	CSI_nRST	Camera Reset Control
JT1201 (23)	HDMI_AUX_N	HDMI auxiliary negative
JT1201 (24)	UART2_TXD	UART 2 TX
JT1201 (25)	HDMI_AUX_P	HDMI auxiliary negative
JT1201 (26)	UART1_RXD	UART 1 RX
JT1201 (27)	GND	Ground
JT1201 (28)	UART2_RXD	UART 2 RX
JT1201 (29)	HDMI_TX1_N	HDMI TX 1 negative
JT1201 (30)	PCIe_nRST	PCIe Reset
JT1201 (31)	HDMI_TX1_P	HDMI TX 1 positive
JT1201 (32)	UART1_TXD	UART 1 TX
JT1201 (33)	GND	Ground

JT1201 (34)	USB2_VBUS	USB 2 VBUS detect
JT1201 (35)	HDMI_TX0_P	HDMI TX 0 positive
JT1201 (36)	USB2_VBUS	USB 2 VBUS detect
JT1201 (37)	HDMI_TX0_N	HDMI TX 0 negative
JT1201 (38)	GND	Ground
JT1201 (39)	GND	Ground
JT1201 (40)	SAI1_RXFS	SAI 1 Receive Frame Sync
JT1201 (41)	HDMI_TX2_N	HDMI TX 2 negative
JT1201 (42)	SAI1_RXD1	SAI 1 RX Data 1
JT1201 (43)	HDMI_TX2_P	HDMI TX 2 positive
JT1201 (44)	SAI1_RXC	SAI 1 RX Clock
JT1201 (45)	GND	Ground
JT1201 (46)	SAI1_RXD0	SAI 1 RX Data 0
JT1201 (47)	HDMI_CLK_P	HDMI Clock positive
JT1201 (48)	SAI1_RXD4	SAI 1 RX Data 4
JT1201 (49)	HDMI_CLK_N	HDMI Clock negative
JT1201 (50)	SAI1_RXD3	SAI 1 RX Data 3
JT1201 (51)	GND	Ground
JT1201 (52)	SAI1_TXFS	SAI 1 TX Frame Sync
JT1201 (53)	AUD_nMUTE	Audio Mute
JT1201 (54)	SAI1_RXD2	SAI 1 RX Data 2
JT1201 (55)	SAI5_RXFS	SAI 5 RX Frame Sync
JT1201 (56)	SAI1_RXD7	SAI 1 RX Data 7
JT1201 (57)	SAI5_RXD0	SAI 5 RX Data 0
JT1201 (58)	SAI1_RXD6	SAI 1 RX Data 6
JT1201 (59)	SAI5_RXD2	SAI 5 RX Data 2
JT1201 (60)	SAI1_RXD5	SAI 1 RX Data 5
JT1201 (61)	SAI5_RXC	SAI 5 RX Clock
JT1201 (62)	SAI1_TXD0	SAI 1 TX Data 0
JT1201 (63)	SAI5_RXD1	SAI 5 RX Data 1
JT1201 (64)	SAI1_TXC	SAI 1 TX Clock
JT1201 (65)	SAI5_RXD3	SAI 5 RX Data 3
JT1201 (66)	SAI1_TXD1	SAI 1 TX Data 1
JT1201 (67)	SAI5_MCLK	SAI 5 Master Clock
JT1201 (68)	SAI1_TXD3	SAI 1 TX Data 3
JT1201 (69)	GND	Ground
JT1201 (70)	SAI1_TXD4	SAI 1 TX Data 4
JT1201 (71)	GND	Ground
JT1201 (72)	SAI1_TXD7	SAI 1 TX Data 7
JT1201 (73)	SAI2_TXC	SAI 2 TX Clock
JT1201 (74)	SAI1_TXD5	SAI 1 TX Data 5

JT1201 (75)	SAI2_RXFS	SAI 2 RX Frame Sync
JT1201 (76)	SAI1_TXD2	SAI 1 TX Data 2
JT1201 (77)	SAI2_RXC	SAI 2 RX Clock
JT1201 (78)	SAI1_TXD6	SAI 1 TX Data 6
JT1201 (79)	SAI2_TXFS	SAI 2 TX Frame Sync
JT1201 (80)	SAI1_MCLK	SAI 1 Master Clock
JT1201 (81)	SAI2_MCLK	SAI 2 Master Clock
JT1201 (82)	GND	Ground
JT1201 (83)	SAI2_RXD	SAI 2 RX Data
JT1201 (84)	MIPI_DSI_LANE1_P	MIPI DSI data lane 1 positive
JT1201 (85)	SAI2_TXD	SAI 2 TX Data
JT1201 (86)	MIPI_DSI_LANE1_N	MIPI DSI data lane 1 negative
JT1201 (87)	GND	Ground
JT1201 (88)	GND	Ground
JT1201 (89)	MIPI_DSI_CLK_P	MIPI DSI clock positive
JT1201 (90)	MIPI_DSI_LANE0_P	MIPI DSI data lane 0 positive
JT1201 (91)	MIPI_DSI_CLK_N	MIPI DSI clock negative
JT1201 (92)	MIPI_DSI_LANE0_N	MIPI DSI data lane 0 negative
JT1201 (93)	GND	Ground
JT1201 (94)	GND	Ground
JT1201 (95)	MIPI_DSI_LANE3_P	MIPI DSI data lane 3 positive
JT1201 (96)	MIPI_DSI_LANE2_P	MIPI DSI data lane 2 positive
JT1201 (97)	MIPI_DSI_LANE3_N	MIPI DSI data lane 3 negative
JT1201 (98)	MIPI_DSI_LANE2_N	MIPI DSI data lane 2 negative
JT1201 (99)	GND	Ground
JT1201 (100)	GND	Ground
JT1202 (1)	GND	Ground
JT1202 (2)	GND	Ground
JT1202 (3)	PCIE2_RX_N	PCIe 2 RX negative
JT1202 (4)	PCIE2_TX_P	PCIe 2 TX positive
JT1202 (5)	PCIE2_RX_P	PCIe 2 RX positive
JT1202 (6)	PCIE2_TX_N	PCIe 2 TX negative
JT1202 (7)	GND	Ground
JT1202 (8)	GND	Ground
JT1202 (9)	USB1_SS_SEL	USB 1 Super Speed Select
JT1202 (10)	PCIE2_REF_CLK_P	PCIe 2 Reference Clock positive
JT1202 (11)	ENET_TX_CTL	Ethernet TX Control
JT1202 (12)	PCIE2_REF_CLK_N	PCIe Reference Clock negative
JT1202 (13)	TCPC_nINT	Type-C Port Controller Interrupt
JT1202 (14)	GND	Ground
JT1202 (15)	BT_DEV_WAKE	Bluetooth Device Wake

JT1202 (16)	NAND_DATA_0	NAND Data 0
JT1202 (17)	SD2_CLK	SD 2 Clock
JT1202 (18)	QSPIA_SCLK	QSPIA Clock
JT1202 (19)	SD2_nCD	SD 2 Chip Detect
JT1202 (20)	NAND_DATA_2	NAND Data 2
JT1202 (21)	SD2_CMD	SD 2 Command
JT1202 (22)	NAND_DATA_1	NAND Data 1
JT1202 (23)	SDIO_WAKE	SDIO Wake
JT1202 (24)	NAND_DATA_5	NAND Data 5
JT1202 (25)	SD2_DATA3	SD 2 Data 3
JT1202 (26)	NAND_DATA_3	NAND Data 3
JT1202 (27)	SD2_DATA0	SD 2 Data 0
JT1202 (28)	QSPIA_nSS0	QSPI Chip Select
JT1202 (29)	SD2_DATA1	SD 2 Data 1
JT1202 (30)	NAND_DATA_7	NAND Data 7
JT1202 (31)	SD2_DATA2	SD 2 Data 2
JT1202 (32)	NAND_DATA_6	NAND Data 6
JT1202 (33)	SD2_nRST	SD 2 Reset
JT1202 (34)	NAND_DATA_4	NAND Data 4
JT1202 (35)	GND	Ground
JT1202 (36)	GND	Ground
JT1202 (37)	ENET_MDIO	Ethernet Management Data Line
JT1202 (38)	GND	Ground
JT1202 (39)	SYS_nRST	Reset input signal
JT1202 (40)	BT_REG_ON	Bluetooth Regulator On
JT1202 (41)	ENET_TXC	Ethernet TX Clock
JT1202 (42)	NAND_nCE3	NAND Chip Enable
JT1202 (43)	ENET_RXC	Ethernet RX Clock
JT1202 (44)	NAND_nWP	NAND Write Protect
JT1202 (45)	ENET_MDC	Ethernet Management Data Clock
JT1202 (46)	NAND_nWE	NAND Write Enable
JT1202 (47)	ENET_RD3	Ethernet Receive Data 3
JT1202 (48)	NAND_nREADY	NAND Ready/Busy
JT1202 (49)	ENET_RD2	Ethernet Receive Data 2
JT1202 (50)	GND	Ground
JT1202 (51)	VDD_PHY_1V8	1.8V HDMI PHY Pull Up Voltage rail
JT1202 (52)	ENET_WoL	Ethernet Wake on LAN
JT1202 (53)	NVCC_SD2	SD 2 Voltage rail
JT1202 (54)	GND	Ground
JT1202 (55)	NVCC_ENET_2V5	2.5V Ethernet Reference Voltage Rail
JT1202 (56)	PCIE2_nCLKREQ	PCIE 2 Clock Request

JT1202 (57)	GND	Ground
JT1202 (58)	GND	Ground
JT1202 (59)	ONOFF	Power ON/OFF signal
JT1202 (60)	GND	Ground
JT1202 (61)	ENET_RX_CTL	Ethernet RX Control
JT1202 (62)	GND	Ground
JT1202 (63)	ENET_RD1	Ethernet Receive Data 1
JT1202 (64)	GND	Ground
JT1202 (65)	ENET_TD1	Ethernet Transmit Data 1
JT1202 (66)	GND	Ground
JT1202 (67)	ENET_TD0	Ethernet Transmit Data 0
JT1202 (68)	GND	Ground
JT1202 (69)	ENET_TD3	Ethernet Transmit Data 3
JT1202 (70)	GND	Ground
JT1202 (71)	ENET_RD0	Ethernet Receive Data 0
JT1202 (72)	GND	Ground
JT1202 (73)	ENET_TD2	Ethernet Transmit Data 2
JT1202 (74)	GND	Ground
JT1202 (75)	GND	Ground
JT1202 (76)	VDD_1V8	1.8V Voltage Rail
JT1202 (77)	PG_SEQ0	Power Good Signal Input
JT1202 (78)	VDD_1V8	1.8V Voltage Rail
JT1202 (79)	VDD_3V3	3.3V Voltage Rail
JT1202 (80)	GND	Ground
JT1202 (81)	ENET_nINT	Ethernet System Interrupt Output
JT1202 (82)	GND	Ground
JT1202 (83)	ENET_nRST	Ethernet System Reset
JT1202 (84)	I2C3_SCL	I2C 3 Clock
JT1202 (85)	GND	Ground
JT1202 (86)	I2C3_SDA	I2C 3 Data
JT1202 (87)	POR_B	Power On Reset
JT1202 (88)	SAI3_TXFS	SAI 3 TX Frame Sync
JT1202 (89)	GND	Ground
JT1202 (90)	SAI3_RXFS	SAI 3 RX Frame Sync
JT1202 (91)	VDD_3V3	3.3V Voltage Rail
JT1202 (92)	SAI3_TXD	SAI 3 Transmit Data
JT1202 (93)	VDD_3V3	3.3V Voltage Rail
JT1202 (94)	SAI3_MCLK	SAI 3 Master Clock
JT1202 (95)	GND	Ground
JT1202 (96)	SAI3_RXD	SAI 3 Receive Data
JT1202 (97)	GND	Ground

JT1202 (98)	SAI3_TXC	SAI 3 Transmit Clock
JT1202 (99)	GND	Ground
JT1202 (100)	SAI3_RXC	SAI 3 Receive Clock

4.3 Wi-Fi/BT Antenna Port Specifications

Parameter	Value	Notes
Connector type	Murata MM4829-2702	MH4 type connector
Port impedance	50 ohms	

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

The input power to the SOM must be provided by a high current 3.3V regulator. This main voltage rail enters the PF4210, which then distributes power via LDOs and switching power supplies. Since these input sources are susceptible to external factors, the following table shows the absolute maximum ratings in which the PF4210 can be exposed to without experiencing functional failure.

Table 3 - Absolute Maximum Input Voltage Rating

Parameter	Max	Units
DC power input (SOM_SYS_PWR), main 3.3V regulator	+3.6	V

5.2 Recommended Operating Conditions

According to component datasheet values, the operating conditions outline the parameters in which a user can control the behaviour of the SOM. If used within the following conditions as outlined in and below, the SOM will meet all performance specifications listed in section 5.2, unless otherwise noted (provided the absolute maximum ratings have never been exceeded).

Table 4 - Recommended Input Voltage Range

Parameter	Min	Typ	Max	Units
DC power input (SOM_SYS_PWR), main 3.3V regulator	+3.30	+3.37	+3.39	V

5.3 Operating Temperature

The SOM operating temperature ratings listed below are based only on the operating temperature grade of the SOM components. Users should consider the specific environmental conditions in which the final product is used in.

Table 5 - Operating Temperature Range

Parameter	Min	Typ	Max	Units
Overall SOM	0	+25	+70	°C

5.4 Power Consumption

Power consumption tests have been done on the SOM running Android 8 under common operational modes. These results are outlined in the table below. All tests were executed at room temperature and with the default thermal solution that ships with the Open-X 8M development kit. Note that power consumption of the SOM varies depending on the thermal solution used. A different thermal solution may result in allowing the CPU to run at higher average frequency but can cause overall power consumption to increase. Since measurements were taken on the SOM_SYS_PWR rail, the power consumed reflects what the SOM consumes during each scenario.

Table 6 - Power Consumption

Operational Modes	Description	Average	Peak
Boot	Power consumption during boot process	N/A	4.1W
Suspend (Wi-Fi Off)	SOM placed in standby (Wi-Fi Off, Display Off)	0.9W	N/A
Suspend (Wi-Fi On)	SOM placed in standby (Wi-Fi On, Display Off)	1.3W	N/A
Idle (Display On)	SOM is idle (Wi-Fi Off, Display On)	2.3W	2.9W
Idle (Display Off)	SOM is idle (Wi-Fi Off, Display Off)	2.0W	2.1W
Video Playback (1080P)	SOM playing back 1080p video (Wi-Fi Off, Display On)	3.0W	3.6W
Video Playback (4K UHD)	SOM playing back 4K UHD video (Wi-Fi Off, Display On)	3.5W	4.2W
Audio Playback	SOM playing back MP3 audio file (Wi-Fi Off, Display Off)	2.0W	2.8W
Wi-Fi Download	SOM downloading data via Wi-Fi (Display Off)	3.1W	4.4W
Wi-Fi Upload	SOM uploading data via Wi-Fi (Display Off)	2.9W	3.9W
Full Load (All Cores)	SOM running all CPU cores (Wi-Fi Off, Display Off)	3.8W	4.1W
Single Core	SOM running single core (Wi-Fi Off, Display Off)	2.5W	2.7W
Bluetooth	SOM playing music over Bluetooth (Wi-Fi Off, Display Off)	2.6W	3.3W

Note:

To obtain these power consumption measurements, the Power Probe Header J600 on the Open-X 8M Development Kit carrier board (see document R-1) is connected to a data acquisition unit (Keithley 2701). The voltages on the SOM_SYS_PWR sense resistor were captured every few seconds over the test period (typically 30 minutes). The SOM power consumption is then calculated as (where Rsense = 5 milliohms):

$$Psom = Vsom_{pwr_{sense_N}} * \frac{(Vsom_{pwr_{sense_P}} - Vsom_{pwr_{sense_N}})}{Rsense}$$

6. MECHANICAL SPECIFICATIONS

This section describes the key mechanical specifications of the Open-X 8M SOM.

6.1 SOM Mechanical Outline

The outer dimensions of the SOM are 35mm x 55mm. The key inner-dimensions for the SOM relate to connector positioning; these dimensions are called out later in this document.

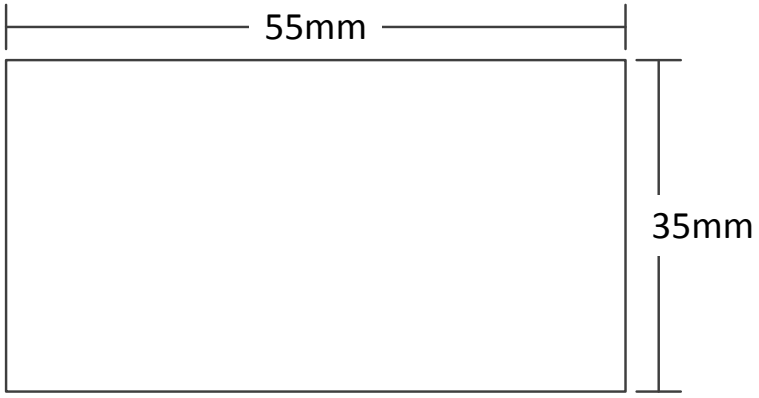

Figure 4 - SOM Mechanical Outline

6.2 Top and Bottom Height Restrictions

The tallest component on the top-side of the SOM is 1.5mm. This height does not include the mating RF antenna cable connectors.

The tallest component on the bottom-side of the SOM is 1.2mm.

6.3 Carrier Board Connector(s)

The Open-X 8M SOM mounts to a carrier board through three (3) board-to-board style connectors. Customers that are designing their own carrier board must ensure that their connector pin outs match the ones on the Open-X 8M development kit carrier board schematic (see R-1).

- SOM-side Connector

Manufacturer	Hirose Electric Co., LTD.
Manufacturer Part Number	DF40C-100DP-0.4V
Type	Header
Pin Count	100
Pin Pitch	0.4mm

- Carrier-side Connector

Manufacturer	Hirose Electric Co., LTD.
Manufacturer Part Number	DF40C-100DS-0.4V
Type	Receptacle
Pin Count	100
Pin Pitch	0.4mm
Minimum Stack Height	1.5mm

Alternate connectors are available, if greater stack heights are desired. The 100-pin DF40C connector is available for stack heights of 1.5mm or 3.0mm. The equivalent Hirose part numbers are listed in the table below.

Hirose Part Number	Stack Height
DF40C-100DS-0.4V	1.5mm
DF40HC(3.0)-100DS-0.4V	3.0mm

Use of multi-connector board to board systems requires consideration of connector footprint and component assembly placement tolerance to optimize carrier board to SOM alignment. Contact Intrinsyc for further guidance.

6.4 Landing Pattern

Dimensions presented are in millimeters (mm). The footprint information in this section is taken from the Open-X 8M Carrier Board and can be used as a guide when designing a landing area for the SOM.

Dimensions show the relative position of each connector on the SOM; referenced to the center of the connector body. An additional figure gives additional dimension information of the connector itself. NOTE: This information is given for reference. It is highly recommended that the Open-X 8M SOM Carrier Board design source files are used to ensure proper dimensioning on any custom carrier board design. For access to the carrier board design files, please contact Intrinsyc sales at https://www.intrinsyc.com/sales-inquiry.

No carrier components (other than the board-to-board connectors) should be placed in the 35.00mm x 55.00mm area occupied by the SOM. It is highly recommended that any non-GND traces be minimized on layer1 (top copper layer) of the carrier in the area occupied by the SOM.

The perspective of these figures is looking thru the SOM to the top-side of the carrier.

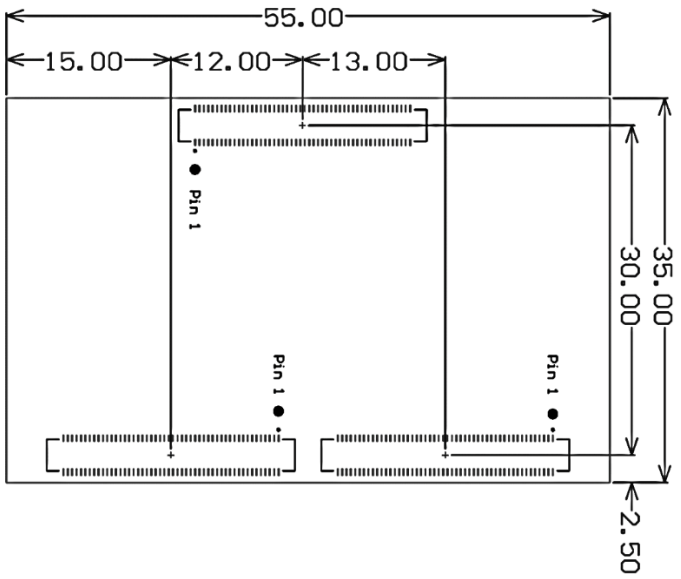

Figure 5 - SOM Land-Pattern Dimensions (mm)

6.5 Weight

The SOM weights 11 grams.

7. PRODUCT MARKING, ORDERING, AND SHIPPING INFO

7.1 Product Marking

The Open-X 8M SOM will have a serial number associated with the board. This serial number will be printed on a small label and placed on the board. The below image is an example of the label:

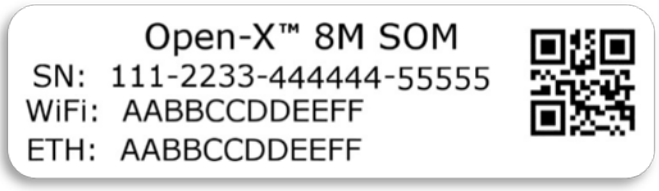

Figure 6 - Open-X 8M SOM Label

Line	Marking	Description/ Notes
1	Open-X™ 8M SOM	Intrinsyc Technologies product name
2	Serial Number	111 = Product number 22 = PCB revision number 33 = BOM revision number 444444 = Date of manufacture (mm/dd/yy) 55555 = Unique serial number for PCB
3	Mac Address	12 hexadecimal digit MAC address
4	Mac Address	12 hexadecimal digit MAC address

7.2 Product Ordering Information

Orderable Part Number	
Open-X 8M SOM	QC-DB-Q00004

The Open-X 8M SOM can be ordered for evaluation and prototype use from the Intrinsyc online store at http://shop.intrinsyc.com. For production orders in volume, or for custom requirements please contact Intrinsyc sales at https://www.intrinsyc.com/sales-inquiry.

7.3 Packaging and Shipping Information

The Open-X 8M SOM is packaged individually in small anti-static bags and bubble-wrap bags for protection during shipping. They are then put into different sized boxes depending upon the quantity of the order. Small quantities are shipped in standard courier boxes with bubble-wrap protection and large quantity orders are packaged in a carton with dividers. See the images below for examples.

Figure 7 - Individual SOM Packaging

Figure 8 - Packaging for Large Quantity Shipments

8. HANDLING PRECAUTIONS

8.1 ESD Precautions

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

The SOM has no ESD protection, it should be handled only in a static-safe environment.

8.2 SOM – Carrier Board Mating Cautions

Caution must be taken when connecting or disconnecting the SOM to a carrier board to prevent damage. Ensure that the SOM is inserted and removed straight up and down to prevent any sideways force on the connectors which could damage them.

The DF40C-100DX board to board connectors are rated for a maximum of 30 mating / un-mating cycles. Caution should be taken when connecting the SOM to these board to board connectors.

8.3 Storage

The SOM must be stored in an antistatic bag.

9. CERTIFICATION

9.1 Radio Certification

The Intrinsyc Open-X 8M SOM uses a pre-certified WLAN/BT module. The module is certified with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth.

FCC ID: 2AFDI-ITCNFA324.

Industry Canada ID: 9049A-ITCNFA324

Further information about the modular certification and requirements for use in an end product is available in the *ITCNFA324 Module Certification OEM Integrator Instructions*, which is available on the Open-X 8M Tech Portal at http://tech.intrinsyc.com (product registration required).

9.2 RoHS / REACH Compliance

The Open-X 8M SOM complies with RoHS and REACH requirements. Certificates of Compliance are available on the Open-X 8M Tech Portal at http://tech.intrinsyc.com (product registration required).

10. WARRANTY TERMS

SOMs that are purchased without a supply agreement as evaluation or development devices have no warranty. SOMs for production use must be purchased through a supply agreement. Please contact Intrinsyc sales for more information on setting up a supply agreement.

https://www.intrinsyc.com/sales-inquiry/

For any warranty and RMA related issues please visit the link below:

https://helpdesk.intrinsyc.com/portal/home

11. COMPANY CONTACT

For more information, support or sales, please contact us.

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Information:

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Product Technical Portal:

http://tech.intrinsyc.com